Experiment 10

Determination of Q-Point for Fixed, Self and Voltage Divider Bias Configuration of JFET Circuits

Objective:

To analyze the fixed, self and voltage Divider bias JFET networks

Introduction:

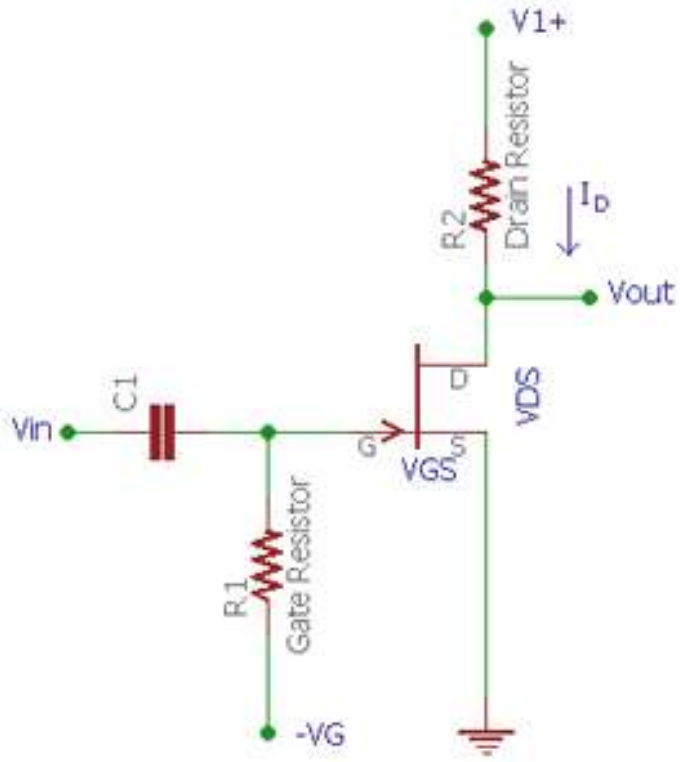
In electronics, Biasing is the setting of initial operating conditions (current and voltage) of an active device in an amplifier. Many electronic devices, such as diodes, transistors and vacuum tubes, whose function is processing time-varying (AC) signals, also require a steady (DC) current or voltage at their terminals to operate correctly. This current or voltage is a bias. The AC signal applied to them is super-positioned on this DC bias current or voltage. For proper working of a transistor, it is essential to apply external voltages of correct polarity across its emitter-base and collector-base junctions. This is transistor biasing. Unlike BJTs, thermal runaway does not occur with FETs. However, the wide differences in maximum and minimum transfer characteristics make ID levels unpredictable with simple fixed-gate bias voltage. To obtain reasonable limits on quiescent drain currents ID and drain-source voltage VDS, source resistor and potential divider bias techniques must be used. With few exceptions, MOSFET bias circuits are similar to those used for JFETs. Various FET biasing circuits in printed circuit board (PCB) design, fabrication and assembly are discussed below.

Biasing of JFET

Different types of techniques are used to bias the JFET in a proper manner. From various techniques, below three are widely used:

- Fixed DC Biasing Technique
- Self-Biasing Technique
- Potential Divider Biasing

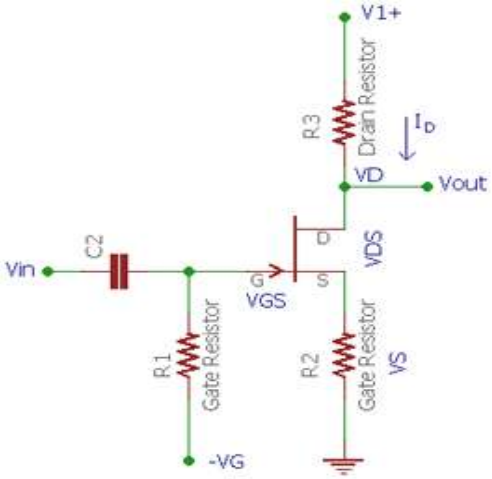
Fixed DC Biasing Technique



In fixed DC biasing technique of an N channel JFET, the gate of the JFET is connected in such a way that the V_{GS} of the JFET remains negative all the time. As the input impedance of a JFET is very high there are no loading effects observed in the input signal. The current flow through the resistor R1 remains zero.

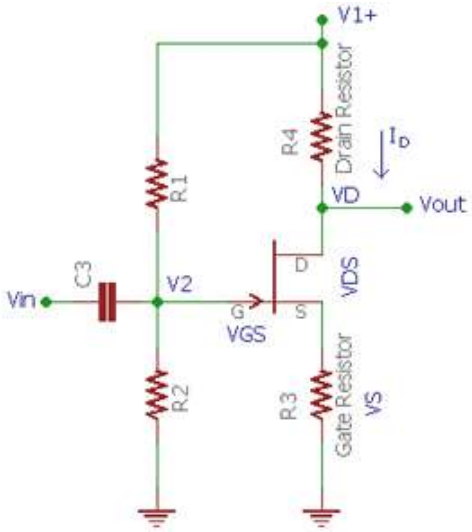
When we apply an AC signal across the input capacitor C1, the signal appears across the gate. Now, if we calculate the voltage drop across the R1, as per the Ohms law it will be V = I x R or V_{drop} = Gate current x R1. As the current flowing to the gate is 0 the Voltage drop across the gate remains zero. So, by this biasing technique, we can control the JFET drain current by just changing the fixed voltage thus changing the V_{GS}.

Self-Biasing Technique



In self-biasing technique, a single resistor is added across the source pin. The voltage drop across the source resistor R2 creates the V_{GS} to bias the voltage. In this technique, the gate current is zero again. The source voltage is determined by the same ohms law V = I x R. Therefore, source voltage = Drain current x source resistor. Now, the gate to source voltage can be determined by the differences between gate voltage and source voltage. Since the gate voltage is 0 (as the gate current flow is 0, as per V = IR, gate voltage = Gate current x gate resistor = 0) the V_{GS} = 0 – Gate current x Source resistance. Thus there is no external biasing source is needed. The biasing is created by self, using the voltage drop across source resistor.

Potential Divider Biasing



In this technique, an additional resistor is used and the circuit is slightly modified from the self-biasing technique, a potential voltage divider using R1 and R2 provide the required DC biasing for the JFET. The voltage drop across the source resistor is needed to be larger than the resistor divider gate voltage. In such a way the V_{GS} remain negative.

Lab Task:

Task: 01

Construct a circuit in fixed Biased Configuration using 2N4416 transistor in which Supply voltage at gate will be -12V Gate Terminal will be connected with 1MΩ potentiometer. RD will be 1KΩ. Find VP and IDSS by varying 1MΩ potentiometer.

Circuit:

Vp =

IDSS =

Task: 02

Calculate and measure ID for specific value of VGS using ID formula.

$$ID = IDSS \times (1 - \frac{VGS}{Vp})^2$$

Calculated:

ID =

Measured:

VRD =

ID =

Task: 03

Construct a circuit in Self Biased Configuration using 2N4416 transistor in which Supply voltage at gate will be GND. Gate Terminal will be connected with 10MΩ resistor. RD will be 1KΩ and RS will be 1.2kΩ. Calculate the value of ID using measured value of VGS.

Circuit:

VGS (measured) =

VD (measured) =

VDS (measured) =

ID (calculated) =

Task: 04

Construct a circuit in voltage divider Biased Configuration using 2N4416 transistor in which Supply voltage at gate will be voltage divider configuration of 10kΩ and 3kΩ resistors. VDD for this circuit is 15V. RD will be 1KΩ and RS will be 1.2kΩ. Calculate the value of ID using measured value of VGS.

Circuit:

VGS (measured) =

VD (measured) =

VDS (measured) =

ID (calculated) =

Lab Exercise and Summary

Summary should cover Introduction, Procedure, Data Analysis and Evaluation.

Student's Signature: _____ **Date: _____**

LABORATORY SKILLS ASSESMENT (Psychomotor)

Total Marks: 100

Criteria (Max Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S< 70%	Level 3 70% ≤ S< 90%	Level 4 90%≤ S ≤100%	Score (S)
Procedural Awareness (20)	Selects inappropriate skills and/or strategies required by the task	Selects and applies appropriate skills and/or strategies required by the task with some errors	Selects and applies the appropriate strategies and/or skills specific to the task without significant errors	Selects and applies appropriate strategies and/or skills specific to the task without any error	
Practical Implementation (30)	Makes several critical errors in applying procedural knowledge related to Determination of Q-Point for Fixed, Self and Voltage Divider Bias Configuration of JFET Circuits	Makes few critical errors in applying procedural knowledge related to Determination of Q-Point for Fixed, Self and Voltage Divider Bias Configuration of JFET Circuits	Makes some non-critical errors in applying procedural knowledge related to DC Analysis of Junction Field Effect Transistor (Determination of Q-Point for Fixed, Self and Voltage Divider Bias Configuration of JFET Circuits	Applies the procedural knowledge in perfect ways related to Determination of Q-Point for Fixed, Self and Voltage Divider Bias Configuration of JFET Circuits	
Safety (10)	Requires constant reminders to follow safety procedures	Requires some reminders to follow safety procedures	Follows safety procedures with only minimal reminders	Routinely follows safety procedures	
Use of Tool/Equipment (20)	Uses tools, equipment and materials with limited competence	Uses tools, equipment and materials with some competence	Uses tools, equipment and materials with considerable competence	Uses tools, equipment and materials with a high degree of competence	
Participation to Achieve Group Goals (10)	Shows little commitment to group goals and fails to perform assigned roles	Demonstrates commitment to group goals, but has difficulty performing assigned roles	Demonstrates commitment to group goals and carries out assigned roles effectively	Actively helps to identify group goals and works effectively to meet them in all roles assumed	
Interpersonal Skills in Group Work (10)	Rarely interacts positively within a group, even with prompting	Interacts with other group members if prompted	Interacts with all group members spontaneously	Interacts positively with all group members and encourages such interaction in others	
				Marks Obtained	

Instructor's Signature: _____ **Date: _____**

LABORATORY SKILLS ASSESMENT (Affective)

Total Marks: 40

Criteria (Max. Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S < 70%	Level 3 70% ≤ S < 90%	Level 4 90% ≤ S ≤ 100%	Score (S)
Introduction (5)	Very little background information provided or information is incorrect	Introduction is brief with some minor mistakes	Introduction is nearly complete, missing some minor points	Introduction complete and well-written; provides all necessary background principles for the experiment	
Procedure (5)	Many stages of the procedure are not entered on the lab report.	Many stages of the procedure are entered on the lab report.	The procedure could be more efficiently designed but most stages of the procedure are entered on the lab report.	The procedure is well designed and all stages of the procedure are entered on the lab report.	
Data Record (10)	Data is brief and missing significant pieces of information.	Data provides some significant information and has few critical mistakes.	Data is almost complete but has some minor mistakes.	Data is complete and relevant. Tables with units are provided. Graphs are labeled. All questions are answered correctly.	
Data Analysis (10)	Data is presented in very unclear manner. Error analysis is not included.	Data is presented in ways (charts, tables, graphs) that are not clear enough. Error analysis is included.	Data is presented in ways (charts, tables, graphs) that can be understood and interpreted. Error analysis is included.	Data are presented in ways (charts, tables, graphs) that best facilitate understanding and interpretation. Error analysis is included.	
Report Quality (10)	Report contains many errors.	Report is somewhat organized with some spelling or grammatical errors.	Report is well organized and cohesive but contains some grammatical errors.	Report is well organized and cohesive and contains no grammatical errors. Presentation seems polished.	
				Marks Obtained	

LABORATORY SKILLS ASSESSMENT (Cognitive)

Total Marks: 10

(If any) **Marks Obtained**	

Instructor's Signature: _____ **Date: _____**