Experiment 12

AC Analysis of Common Source JFET Amplifier

OBJECTIVE:

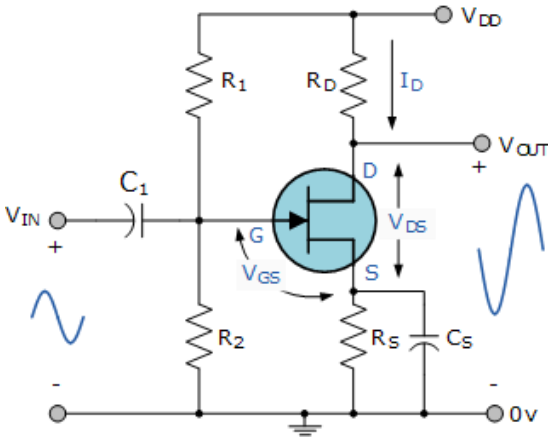
To implement Junction Field Effect Transistor (JFET) as an amplifier.

Introduction:

Common Source JFET Amplifier uses junction field effect transistors as its main active device offering high input impedance characteristics Transistor amplifier circuits such as the common emitter amplifier are made using Bipolar Transistors, but small signal amplifiers can also be made using Field Effect Transistors. These devices have the advantage over bipolar transistors of having an extremely high input impedance along with a low noise output making them ideal for use in amplifier circuits that have very small input signals.

The design of an amplifier circuit based around a junction field effect transistor or "JFET", (N-channel FET for this tutorial) or even a metal oxide silicon FET or "MOSFET" is exactly the same principle as that for the bipolar transistor circuit. Firstly, a suitable quiescent point or "Q-point" needs to be found for the correct biasing of the JFET amplifier circuit with single amplifier configurations of Common-source (CS), Common-drain (CD) or Source-follower (SF) and the Common-gate (CG) available for most FET devices. These three JFET amplifier configurations correspond to the common-emitter, emitter-follower and the common-base configurations using bipolar transistors. In this tutorial about FET amplifiers we will look at the popular **Common Source JFET Amplifier** as this is the most widely used JFET amplifier design. Consider the Common Source JFET Amplifier circuit configuration below.

Common Source JFET Amplifier



The amplifier circuit consists of an N-channel JFET, but the device could also be an equivalent N-channel depletion-mode MOSFET as the circuit diagram would be the same just a change in the FET, connected in a common source configuration. The JFET gate voltage Vg is biased through the potential divider network set up by resistors R1 and R2 and is biased to operate within its saturation region which is equivalent to the active region of the bipolar junction transistor.

Unlike a bipolar transistor circuit, the junction FET takes virtually no input gate current allowing the gate to be treated as an open circuit. Then no input characteristics curves are required. We can compare the JFET to the bipolar junction transistor (BJT) in the following table.

JFET to BJT Comparison

Junction FET	Bipolar Transistor
Gate (G)	Base (B)
Drain (D)	Collector (C)
Source (S)	Emitter (E)
Gate Supply ($\boldsymbol{V_G}$)	Base Supply ($\boldsymbol{V_B}$)
Drain Supply ($\boldsymbol{V_{DD}}$)	Collector Supply ($\boldsymbol{V_{CC}}$)
Drain Current ($\boldsymbol{I_D}$)	Collector Current ($\boldsymbol{I_C}$)

Since the N-Channel JFET is a depletion mode device and is normally "ON", a negative gate voltage with respect to the source is required to modulate or control the drain current. This negative voltage can be provided by biasing from a separate power supply voltage or by a self-biasing arrangement as long as a steady current flows through the JFET even when there is no input signal present and Vg maintains a reverse bias of the gate-source pn junction.

In our simple example, the biasing is provided from a potential divider network allowing the input signal to produce a voltage fall at the gate as well as voltage rise at the gate with a sinusoidal signal. Any suitable pair of resistor values in the correct proportions would produce the correct biasing voltage so the DC gate biasing voltage Vg is given as:

$$V_G = \frac{V_{DD}\,R_2}{R_1 + R_2} = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

Note that this equation only determines the ratio of the resistors R1 and R2, but in order to take advantage of the very high input impedance of the JFET as well as reducing the power dissipation within the circuit, we need to make these resistor values as high as possible, with values in the order of 1MΩ to 10MΩ being common.

The input signal, (Vin) of the common source JFET amplifier is applied between the Gate terminal and the zero volts rail, (0v). With a constant value of gate voltage Vg applied the JFET operates within its "Ohmic region" acting like a linear resistive device. The drain circuit contains the load resistor, Rd. The output voltage, Vout is developed across this load resistance.

The efficiency of the common source JFET amplifier can be improved by the addition of a resistor, Rs included in the source lead with the same drain current flowing through this resistor. Resistor, Rs is also used to set the JFET amplifiers "Q-point".

When the JFET is switched fully "ON" a voltage drop equal to Rs*Id is developed across this resistor raising the potential of the source terminal above 0v or ground level. This voltage drop across Rs due to the drain current provides the necessary reverse biasing condition across the gate resistor, R2 effectively generating negative feedback.

So in order to keep the gate-source junction reverse biased, the source voltage, Vs needs to be higher than the gate voltage, Vg. This source voltage is therefore given as:

$$V_S = I_D \times R_S = V_G - V_{GS}$$

Then the Drain current, Id is also equal to the Source current, Is as "No Current" enters the Gate terminal and this can be given as:

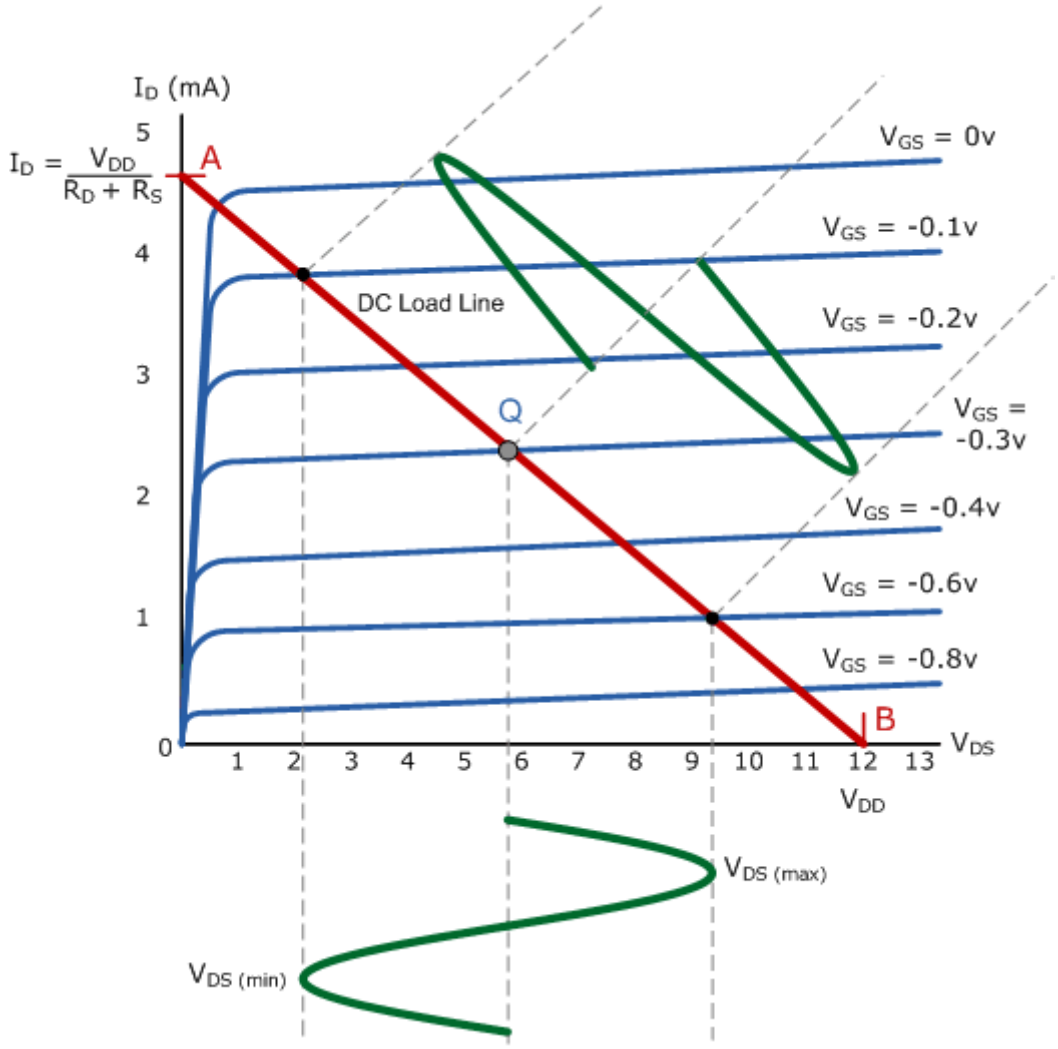
$$I_D = \frac{V_S}{R_S} = \frac{V_{DD}}{R_D + R_S}$$

This potential divider biasing circuit improves the stability of the common source JFET amplifier circuit when being fed from a single DC supply compared to that of a fixed voltage biasing circuit. Both resistors Rs and the source by-pass capacitor, Cs serve basically the same function as the emitter resistor and capacitor in the common emitter bipolar transistor amplifier circuit, namely to provide good stability and prevent a reduction in the loss of the voltage gain. However, the price paid for a stabilized quiescent gate voltage is that more of the supply voltage is dropped across Rs.

The value in farads of the source by-pass capacitor is generally fairly high above 100uF and will be polarized. This gives the capacitor an impedance value much smaller, less than 10% of the transconductance, gm (the transfer coefficient representing gain) value of the device. At high frequencies the by-pass capacitor acts essentially as a short-circuit and the source will be effectively connected directly to ground.

The basic circuit and characteristics of a **Common Source JFET Amplifier** are very similar to that of the common emitter amplifier. A DC load line is constructed by joining the two points relating to the drain current, Id and the supply voltage, Vdd remembering that when Id = 0: (Vdd = Vds) and when Vds = 0: (Id = Vdd/R_L). The load line is therefore the intersection of the curves at the Q-point as follows.

Common Source JFET Amplifier Characteristics Curves



As with the common emitter bipolar circuit, the DC load line for the common source JFET amplifier produces a straight line equation whose gradient is given as: -1/(Rd + Rs) and that it

crosses the vertical Id axis at point A equal to Vdd/(Rd + Rs). The other end of the load line crosses the horizontal axis at point B which is equal to the supply voltage, Vdd.

The actual position of the Q-point on the DC load line is generally positioned at the mid center point of the load line (for class-A operation) and is determined by the mean value of Vg which is biased negatively as the JFET is a depletion-mode device. Like the bipolar common emitter amplifier, the output of the **Common Source JFET Amplifier** is 180^{o} out of phase with the input signal.

One of the main disadvantages of using Depletion-mode JFET is that they need to be negatively biased. Should this bias fail for any reason the gate-source voltage may rise and become positive causing an increase in drain current resulting in failure of the drain voltage, Vd.

Also, the high channel resistance, Rds(on) of the junction FET, coupled with high quiescent steady state drain current makes these devices run hot so additional heatsink is required. However, most of the problems associated with using JFET's can be greatly reduced by using enhancement-mode MOSFET devices instead.

MOSFET's or Metal Oxide Semiconductor FET's have much higher input impedance's and low channel resistances compared to the equivalent JFET. Also, the biasing arrangements for MOSFETs are different and unless we bias them positively for N-channel devices and negatively for P-channel devices no drain current will flow, then we have in effect a fail safe transistor.

JFET Amplifier Current and Power Gains

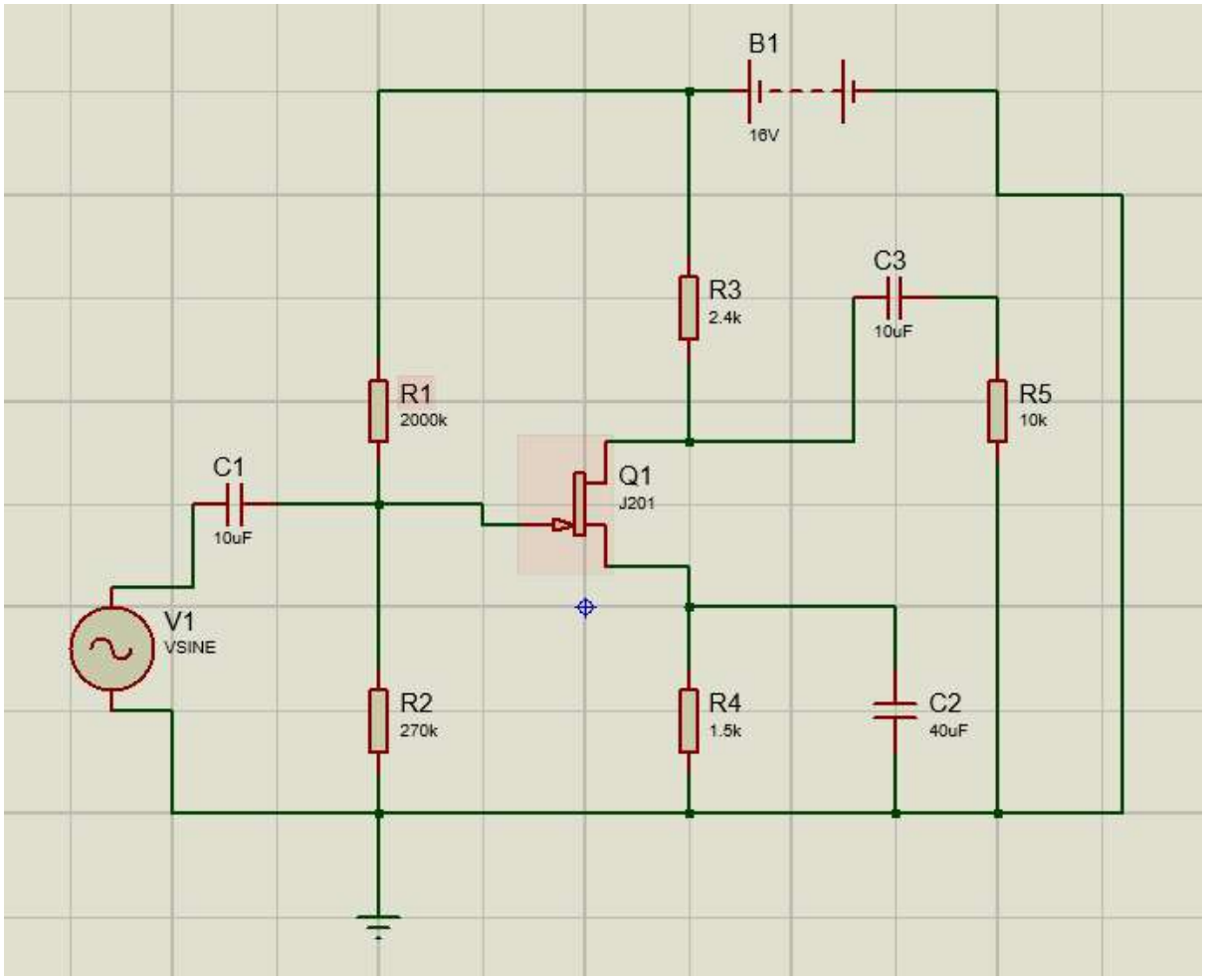
We said previously that the input current, Ig of a common source JFET amplifier is very small because of the extremely high gate impedance, Rg. A common source JFET amplifier therefore has a very good ratio between its input and output impedances and for any amount of output current, I_{OUT} the JFET amplifier will have very high current gain Ai.

Because of this common source JFET amplifiers are extremely valuable as impedance matching circuits or are used as voltage amplifiers. Likewise, because: Power = Voltage x Current, (P = V*I) and output voltages are usually several millivolts or even volts, the power gain, Ap is also very high. In the next tutorial we will look at how the incorrect biasing of the transistor amplifier can cause Distortion to the output signal in the form of amplitude distortion due to clipping and as well as the effect of phase and frequency distortion.

Task:

Construct the circuit given below and plot the input/output waveforms of the amplifier circuit.

VSINE= 25mV peak, frequency= 5K Hz



Lab Exercise and Summary

Summary should cover Introduction, Procedure, Data Analysis and Evaluation.

Student's Signature: _____ **Date: _____**

LABORATORY SKILLS ASSESMENT (Psychomotor)

Total Marks: 100

Criteria (Max Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S< 70%	Level 3 70% ≤ S< 90%	Level 4 90%≤ S ≤100%	Score (S)
Procedural Awareness (20)	Selects inappropriate skills and/or strategies required by the task	Selects and applies appropriate skills and/or strategies required by the task with some errors	Selects and applies the appropriate strategies and/or skills specific to the task without significant errors	Selects and applies appropriate strategies and/or skills specific to the task without any error	
Practical Implementation (30)	Makes several critical errors in applying procedural knowledge related to AC analysis of Common source JFET Amplifier	Makes few critical errors in applying procedural knowledge related to AC analysis of Common source JFET Amplifier	Makes some non-critical errors in applying procedural knowledge related to AC analysis of Common source JFET Amplifier	Applies the procedural knowledge in perfect ways related to AC analysis of Common source JFET Amplifier	
Safety (10)	Requires constant reminders to follow safety procedures	Requires some reminders to follow safety procedures	Follows safety procedures with only minimal reminders	Routinely follows safety procedures	
Use of Tool/Equipment (20)	Uses tools, equipment and materials with limited competence	Uses tools, equipment and materials with some competence	Uses tools, equipment and materials with considerable competence	Uses tools, equipment and materials with a high degree of competence	
Participation to Achieve Group Goals (10)	Shows little commitment to group goals and fails to perform assigned roles	Demonstrates commitment to group goals, but has difficulty performing assigned roles	Demonstrates commitment to group goals and carries out assigned roles effectively	Actively helps to identify group goals and works effectively to meet them in all roles assumed	
Interpersonal Skills in Group Work (10)	Rarely interacts positively within a group, even with prompting	Interacts with other group members if prompted	Interacts with all group members spontaneously	Interacts positively with all group members and encourages such interaction in others	
				Marks Obtained	

Instructor's Signature: _____ **Date: _____**

LABORATORY SKILLS ASSESMENT (Affective)

Total Marks: 40

Criteria (Max. Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S < 70%	Level 3 70% ≤ S < 90%	Level 4 90% ≤ S ≤ 100%	Score (S)
Introduction (5)	Very little background information provided or information is incorrect	Introduction is brief with some minor mistakes	Introduction is nearly complete, missing some minor points	Introduction complete and well-written; provides all necessary background principles for the experiment	
Procedure (5)	Many stages of the procedure are not entered on the lab report.	Many stages of the procedure are entered on the lab report.	The procedure could be more efficiently designed but most stages of the procedure are entered on the lab report.	The procedure is well designed and all stages of the procedure are entered on the lab report.	
Data Record (10)	Data is brief and missing significant pieces of information.	Data provides some significant information and has few critical mistakes.	Data is almost complete but has some minor mistakes.	Data is complete and relevant. Tables with units are provided. Graphs are labeled. All questions are answered correctly.	
Data Analysis (10)	Data is presented in very unclear manner. Error analysis is not included.	Data is presented in ways (charts, tables, graphs) that are not clear enough. Error analysis is included.	Data is presented in ways (charts, tables, graphs) that can be understood and interpreted. Error analysis is included.	Data are presented in ways (charts, tables, graphs) that best facilitate understanding and interpretation. Error analysis is included.	
Report Quality (10)	Report contains many errors.	Report is somewhat organized with some spelling or grammatical errors.	Report is well organized and cohesive but contains some grammatical errors.	Report is well organized and cohesive and contains no grammatical errors. Presentation seems polished.	
				Marks Obtained	

LABORATORY SKILLS ASSESSMENT (Cognitive)

Total Marks: 10

(If any) **Marks Obtained**	

Instructor's Signature: _____ **Date: _____**