# Experiment 3

Analysis of Series and Parallel Connected Diodes

## OBJECTIVE:

- To understand about series and parallel combination of diode.
- To understand and implement the basic logic gates operation using diode.

## Operation:

Diodes are connected inside the circuit in two configurations. These configurations are:

- Series configuration
- Parallel configuration

Both of the connection patterns are widely used will be discuss below:

**Series Configuration:**

Series connection means a side by side connection. When two components are connected in series, they have one common junction. The variation of voltage and current in a series connection is as follows:

- Potential difference across every component is different.
- The current across every component connected in series remains the same.

The same properties also hold true for diodes when they are connected in a series configuration. When connected in series, we observe the following properties to hold true among the diodes:

- Resultant diode's forward voltage increases.
- Reverse blocking capabilities of diodes are increased in series connection.

Consider two diodes connected in series. The thing to be kept in mind over here is that all the diodes connected in series won't have the same characteristics as shown in the graph below.

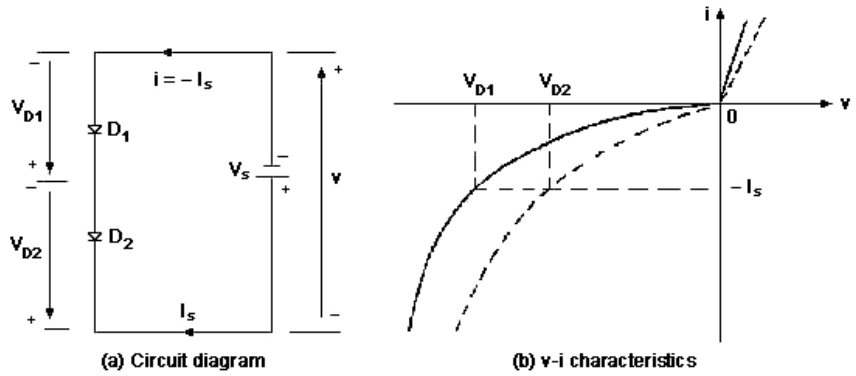



*Figure 3.1 Series connected diode configuration*

V-I characteristics show that the diodes have different blocking voltages. In forward biased state, the voltage drop and the forward current would be same on the diodes. While in the reverse biased the blocking voltage is different as the diodes have to carry the same leakage current.

This problem can be solved by connected resistances across every diode. Voltage would be shared equally; hence the leakage current would differ.

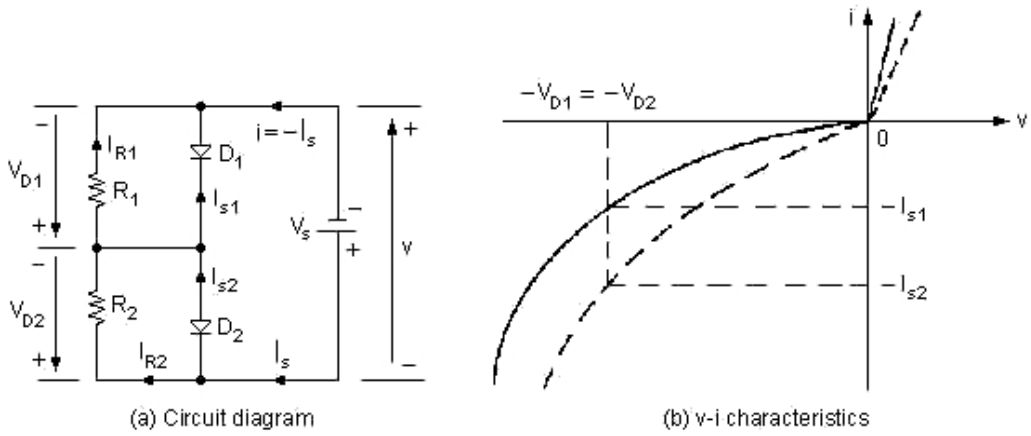



*Figure 3.2 Series connected diode with resistor*

A single diode cannot meet higher voltage requirements, unless it is connected in series. So the major areas of application are:

- HVDC (High voltage direct current) transmission lines.
- Commercial areas where regulated voltage supply is needed.

**Parallel Configuration:**

Parallel connection means the components are connected across each other, having two common points. Current differs across each component while voltage drop is same. When diodes are connected in parallel, this same trend is observed.

- Current carrying capacity increases.
- No conduction in resultant diode in both sides.

Consider two diodes connected in parallel configuration. Current would be shared among the two diodes. To make this sharing equal, inductors (with same inductances) are connected. When current at D1 increases, the voltage drop across L1 increases, generating an opposite polarity value at L2. Inductors are used for dynamic conditions. Inductors are usually bulky and expensive and generate spikes which can cause problems.

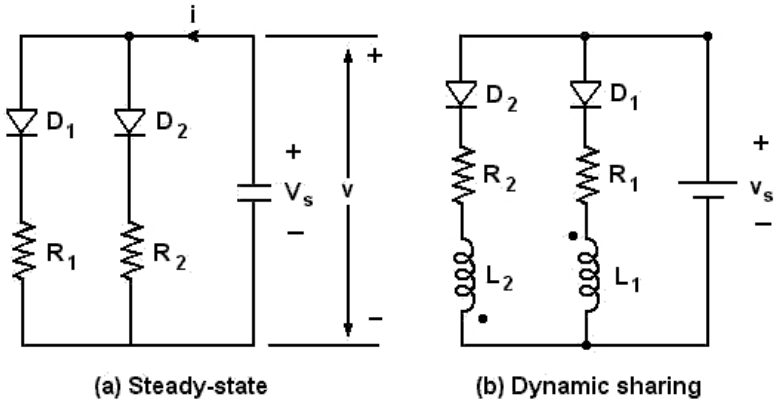



*Figure 3.3 Parallel connected connection of diode*

Diodes of same type having same voltage drops can be used for steady state conditions. In this case, the parallel diodes would have the same reverse blocking voltages. Some precautions are to be kept in mind while using the diodes with same forward voltage drops, which are:

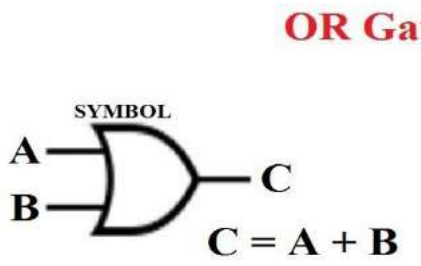
- The diodes should have same heat sinks.
- They should be cooled equally when necessary.

Negligence would change the temperature of the diodes unequally. This will in turn cause the forward characteristics to differ which can create problems.

**Logic Gates:** Logic gates are building blocks of the digital system. In this post, we will see how basic digital gates can be made with the help of diodes. If we need an OR gate we can use

a 4071 OR CMOS IC or a TTL 7432 OR IC. If we need a AND gate we can use a 4081 AND CMOS IC or a TTL 7408 AND IC but sometimes it is easier to use diodes. Diode Logic uses the fact that diodes conduct only in one direction. (they behave like switches).

**OR Gate Using Diodes:**




TRUTH TABLE

| INPUT | | OUTPUT |
|---|---|---|
| A | B | A OR B |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**Figure 3.4: OR Gate**

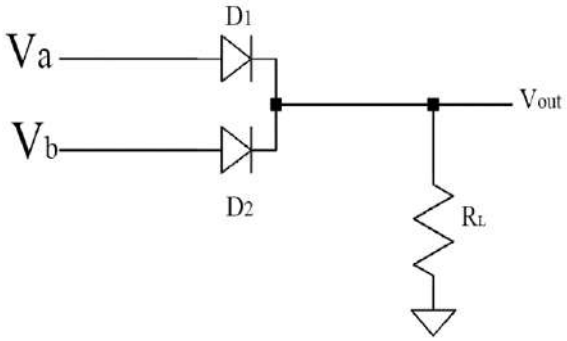



**Figure 3.5: OR Gate Using Diodes**

OR gate has two or more inputs and only one output. The output of the OR gate is HIGH if one or more inputs are HIGH. Circuit diagram of two input, positive logic OR gate using diodes and a resistor is shown above.

In this logic gate circuit, Va and Vb are inputs and Vout is output. These symbols can take only two values either LOW or HIGH.

**Working:**

Let us understand the working of this circuit.

- If all inputs are in LOW, both the diode becomes in reverse biased hence acts as an open switch. Hence the output voltage is 0V.

- If A is HIGH and B is LOW, the diode D1 becomes in forward biased hence act as the closed switch. (Neglecting diode forward resistance and voltage drop across the diode) Hence the output is HIGH.
- Also, If A is LOW and B is HIGH. Diode D2 becomes in forward biased and act as an open switch. Hence the output is HIGH.
- If both the input is in HIGH then the output is equal to the more positive value of the input.

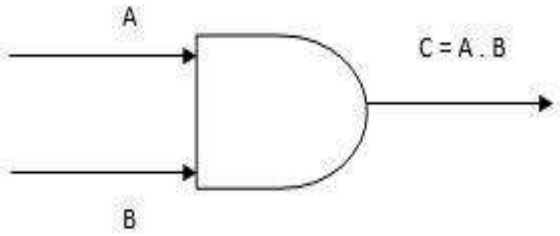
Hence OR function has been implemented.

**AND**

Truth table:

| Input | | Output |
|---|---|---|
| A | B | C = A . B |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Graphical Symbol:




Algebraic Expression is, C = A . B

**Figure 3.6: AND Gate**

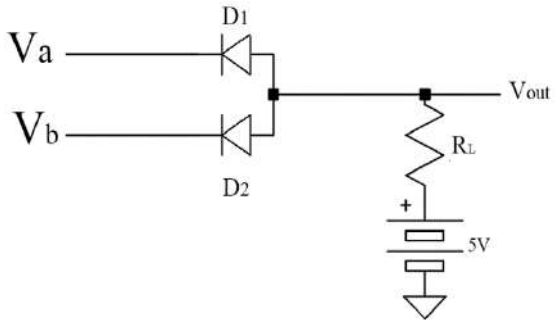



**Figure 3.7: AND Gate Using Diodes**

**Gate Using Diodes:**

AND gate has two or more inputs and only one output. The output of logic AND gate is HIGH if all inputs are HIGH. For other input, the output is LOW. Circuit diagram of two-input OR gate using diodes and a resistor is shown below:

Here Va and Vb are inputs and Vout is output.

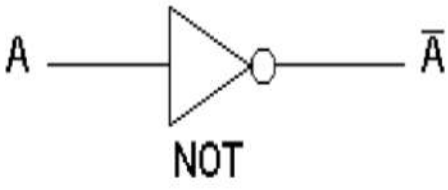
**Working:**

- If A is HIGN and b is LOW, the diode D1 becomes in reversed biased hence act as an open switch. Also, diode D2 becomes in forward biased hence act as the closed switch. Hence the output is LOW.
- If A is LOW and B is HIGH, the diode D1 becomes in forward biased hence act as the closed switch. Also, diode D2 becomes in reversed biased hence act as an open switch. The output is LOW.
- If all inputs are 0 then all diode becomes in forward biased and act as an open switch. Hence the output is LOW.
- When all inputs are HIGH then all diodes become in the reversed biased hence act as an open switch. Hence the output is HIGH.

# Verification of Other Logic Gates

**NOT Gate:**

When input variable A is low the output of a NOT gate is High. The logic symbol of NOT Gate is shown in Figure 6.5. The IC 74LS04 is a single input NOT Gate IC and it consists of 6NOT gates. The IC has 14 pins constructed in Dual in Line package (DIP) as shown in Figure 6.5. The truth table of NOT Gate is as shown in Figure 3.7.



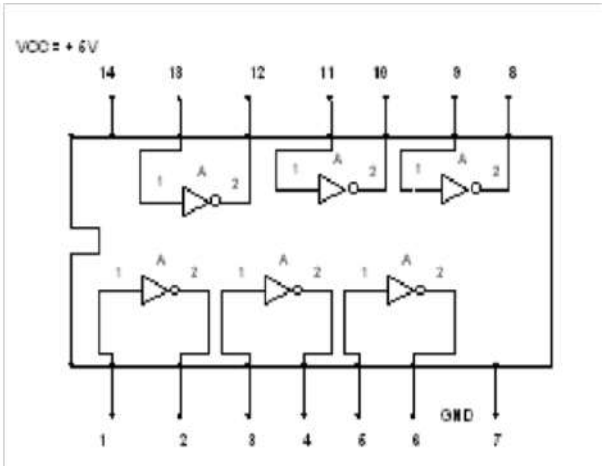




**Figure 3.8: NOT - Gate Symbol**

## NAND Gate:

The outputs of all NAND gates are high if **any** of the inputs are low. The logic symbol of NAND Gate is shown in Figure 3.9. The IC 74 LS00 is a two input NAND Gate IC. It consists 4 NAND gates built in.

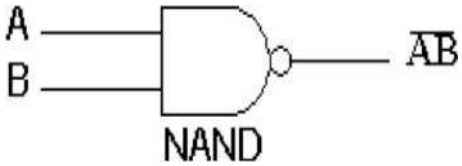
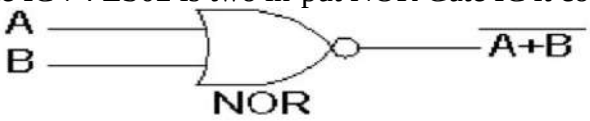



**Figure 3.9: NAND Gate**

## NOR Gate:

The outputs of all NOR gates are low if **any** of the inputs are high. The logic symbol of NOR Gate is shown in Fig. The IC 74 LS02 is two in-put NOR Gate IC it consists of 4 NOR gates.



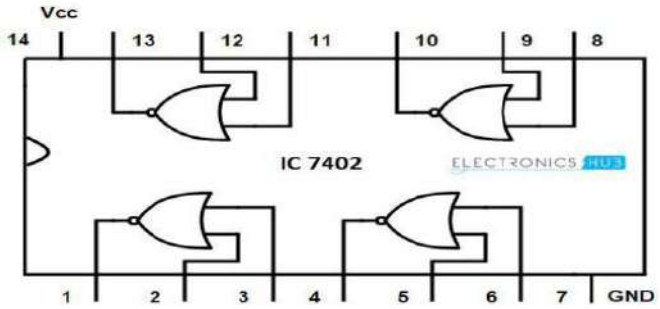




**Figure 3.10: NOR Gate**

## EX-OR Gate:

The '**Exclusive-OR**' gate is a circuit which will give a high output if **either, but not both**, of its two inputs are high. . The logic symbol of **EXOR** Gate is shown in Figure 3.11. The IC 74LS86 is a single input **EXOR** Gate IC and it consists of 4- **EXOR** gates.

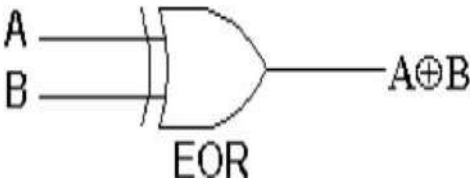



**Figure 3.11: EX-OR Gate**

**EX-NOR Gate:**

The '**Exclusive-NOR**' gate is a circuit which will give a high output if **either, but not both**, of its two inputs are high. . The logic symbol of **EXNOR** Gate is shown in Figure 3.12. The truth table of **EXOR**.

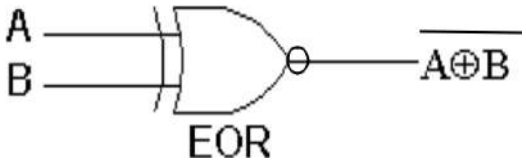



**Figure 3.12: EX-NOR Gate**

## Lab Activities:

**1.** Implement the following circuit on breadboard and find Voltage and current across diodes

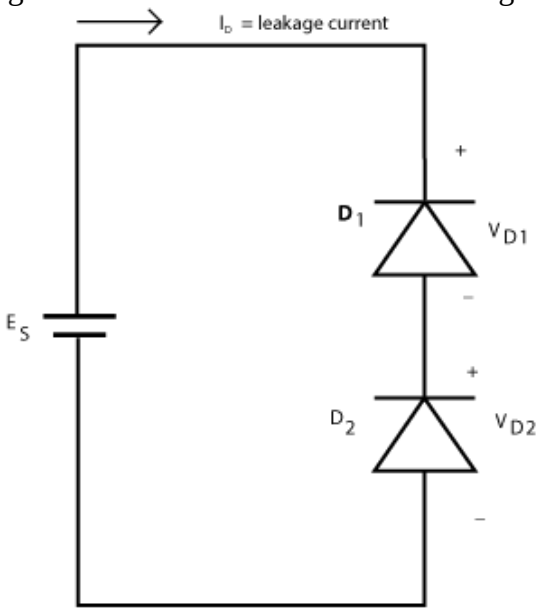


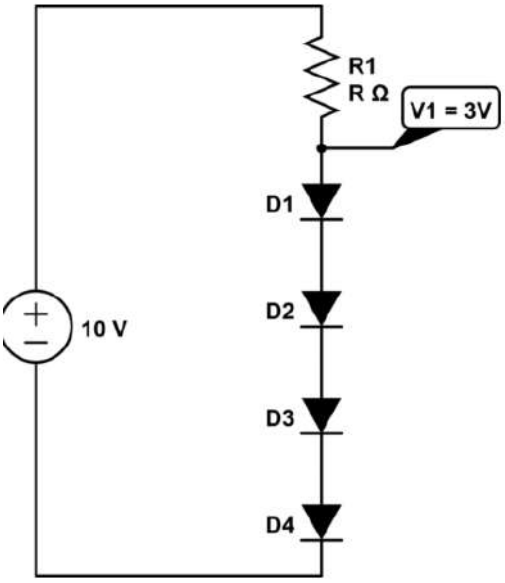

*Figure 3.13 Series connected diode*

$I_D$ = _____

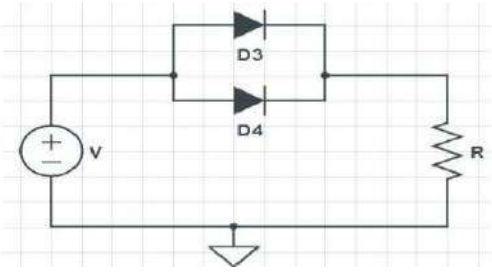
$V_{D1}$ = _____

$V_{D2}$ = _____

**2.** Implement the following circuit on breadboard and verify Voltage V1 and find current across diodes

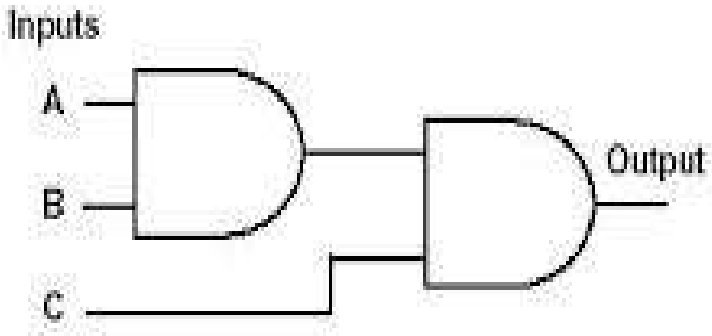


**3.** Implement the following circuit on breadboard and find Voltage and current across diodes



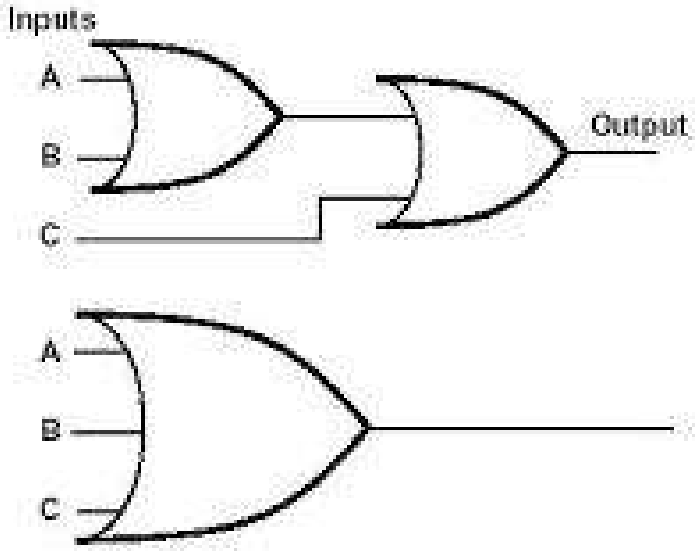

**4.** Implement the following circuit on breadboard also verify their truth table.

**1)**




| A | B | C | Output |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**2)**




| A | B | C | Output |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

# Lab Exercise and Summary

**Summary should cover Introduction, Procedure, Data Analysis and Evaluation.**

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**Student's Signature: _____** **Date: _____**

## LABORATORY SKILLS ASSESSMENT (Psychomotor)

**Total Marks: 100**

| Criteria (Max Marks) | Level 1 0% ≤ S < 50% | Level 2 50% ≤ S< 70% | Level 3 70% ≤ S< 90% | Level 4 90%≤ S ≤100% | Score (S) |
|---|---|---|---|---|---|
| **Procedural Awareness (20)** | Selects inappropriate skills and/or strategies required by the task. | Selects and applies appropriate skills and/or strategies required by the task with major errors. | Selects and applies the appropriate strategies and/or skills specific to the task without significant errors. | Selects and applies appropriate strategies and/or skills specific to the task without any error. | |
| **Practical Implementation (30)** | Makes major critical errors in applying procedural knowledge related to series and parallel connected diodes | Makes numerous critical errors in applying procedural knowledge related to series and parallel connected diodes | Makes some non-critical errors in applying procedural knowledge related to series and parallel connected diodes | Applies the procedural knowledge in optimized ways related to series and parallel connected diodes | |
| **Participation to Achieve Group Goals (10)** | Shows little commitment to achieve group goals and fails to perform assigned roles. | Demonstrates commitment to achieve group goals, but has difficulty in performing assigned roles. | Demonstrates commitment to achieve group goals and carries out assigned roles effectively. | Actively helps to identify, achieve group goals and works effectively to meet them in all roles assumed. | |
| **Interpersonal Skills in Group Work (10)** | Rarely interacts positively within a group, even with prompting. | Interacts with other group members if prompted. | Interacts with all group members spontaneously. | Interacts positively with all group members and encourages such interaction in others. | |
| **Use of Tool/Equipment (20)** | Uses tools, equipment and materials with limited competence. | Uses tools, equipment and materials with some competence. | Uses tools, equipment and materials with considerable competence. | Uses tools, equipment and materials with a high degree of competence. | |
| **Safety (10)** | Requires constant reminders to follow safety procedures. | Requires some reminders to follow safety procedures. | Follows safety procedures with only minimal reminders. | Routinely follows safety procedures. | |
| | | | | **Marks Obtained** | |

**Instructor Name: _____ Sign: _____**

## LABORATORY SKILLS ASSESSMENT (Affective)

**Total Marks: 40**

| Criteria (Max. Marks) | Level 1 0% ≤ S < 50% | Level 2 50% ≤ S < 70% | Level 3 70% ≤ S < 90% | Level 4 90% ≤ S ≤ 100% | Score |
|---|---|---|---|---|---|
| **Introduction (5)** | Very little background information provided or information is incorrect | Introduction is brief with some minor mistakes | Introduction is nearly complete, missing some minor points | Introduction complete and well-written; provides all necessary background principles for the experiment | |
| **Procedure (5)** | Many stages of the procedure are not entered on the lab report. | Many stages of the procedure are entered on the lab report. | The procedure could be more efficiently designed but most stages of the procedure are entered on the lab report. | The procedure is well designed and all stages of the procedure are entered on the lab report. | |
| **Data Record (10)** | Data is brief and missing significant pieces of information. | Data provides some significant information and has few critical mistakes. | Data is almost complete but has some minor mistakes. | Data is complete and relevant. Tables with units are provided. Graphs are labeled. All questions are answered correctly. | |
| **Data Analysis (10)** | Data is presented in very unclear manner. | Data is presented in ways that are not clear enough. | Data is presented in ways that can be understood and interpreted. | Data is presented in ways that best facilitate understanding and interpretation. | |
| **Report Quality (10)** | Report contains many errors. | Report is somewhat organized with some spelling or grammatical errors. | Report is well organized and cohesive but contains some grammatical errors. | Report is well organized and cohesive and contains no grammatical errors. Presentation seems polished. | |
| | | | | **Marks Obtained** | |

## LABORATORY SKILLS ASSESSMENT (Cognitive) Total Marks: 10

| | |
|---|---|
| (If any)<br><br>**Marks Obtained** | |

**Instructor's Signature: _____** **Date: _____**