Experiment No 8

Implementation of D-Type Latch and J-K Flip Flop

8.1 Objectives:

After completing this experiment, student will be able to:

- Describe construction and operational principle of Latches.
- Design and analyze operation of Latches.
- Describe construction and operational principle of Flip-Flop.
- Design and analyze operation of Flip-Flops.

8.2 Background Theory

The digital circuits we have seen so far (gates, multiplexer, demultiplexer, encoders, decoders) are combinatorial in nature, i.e., the output(s) depends only on the present values of the inputs and not on their past values. In sequential circuits, the "state" of the circuit is crucial in determining the output values. For a given input combination, a sequential circuit may produce different output values, depending on its previous state. In other words, a sequential circuit has a memory (of its past state) whereas a combinatorial circuit has no memory. Sequential circuits (together with combinatorial circuits) make it possible to build several useful applications, such as counters, registers, arithmetic/logic unit (ALU), all the way to microprocessors. A memory stores data – usually one bit per element. A snapshot of the memory is called the state. A one bit memory is often called a bistable, i.e., it has 2 stable internal states. Flip-flops and latches are particular implementations of bistables. Main difference between storage elements: Number of inputs they have and how the inputs affect the binary state. There is two main types:

- **Latches** (level-sensitive)
- **Flip-Flops** (edge-sensitive)

There are two types of sequential circuits:

- **Synchronous**: The behavior of the circuit depends on the input signal at discrete instances of time (also called clocked)
- **Asynchronous**: The behavior of the circuit depends on the input signals at any instance of time and the order of the inputs change
    - A combinational circuit with feedback

8.2.1 Latches

Provide us with a simple form of memory State of the circuit depends not only on the current inputs, but also on the recent history of the inputs. Our circuit responds any time the inputs are

low. We want to limit the state change to a very narrow time period. This will allow us to synchronize the state change of several devices.

There are two types of Latches:

- S-R Latch
- D Latch

8.2.1.1 S-R Latch

An RS latch is a memory element with 2 inputs: Reset (R) and Set (S) and 2 outputs **Q** and **Q'**.

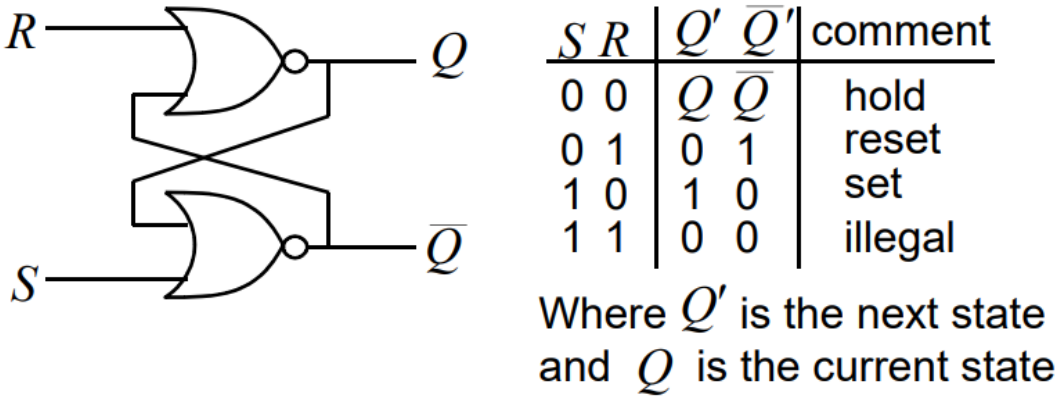


Figure 8.1 S-R Latch Logic Diagram

For the RS latch we have just described, we can see that the output state changes occur directly in response to changes in the inputs. This is called asynchronous operation.

Q	S	R	Q'	comment
0	0	0	0	hold
0	0	1	0	reset
0	1	0	1	set
0	1	1	0	illegal
1	0	0	1	hold
1	0	1	0	reset
1	1	0	1	set
1	1	1	0	illegal

Figure 8.2 R-S Latch State transition Table

8.2.1.2 D Latch

We now modify the RS Latch such that its output state is only permitted to change when a valid enable signal (which could be the system clock) is present. This is achieved by introducing a couple of AND gates in cascade with the R and S inputs that are controlled by an additional input known as the enable (EN) input.

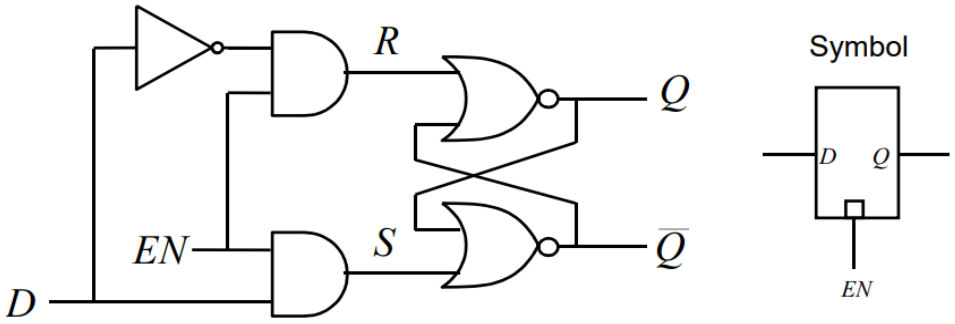


Figure 8.3 D Latch Logic Diagram

The complement function ensures that R and S can never be 1 at the same time, i.e., illegal avoided.

D	EN	Q'	$\overline{Q}'$	comment
X	0	Q	$\overline{Q}$	RS hold
0	1	0	1	RS reset
1	1	1	0	RS set

Figure 8.4 D Latch Input Output Table

A latch is a level sensitive device. **Problem:** A latch is transparent; state keep changing as long as the clock remains active. Due to this uncertainty, latches cannot be reliably used as storage elements.

8.2.2 Flip-Flop

A flip flop is an electronic circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying inputs. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems. Both are used as data storage elements. It is the basic storage element in sequential logic. But first, let's clarify the difference between a latch and a flip-flop.

There are 4 types of Flip-Flops:

- S-R Flip-Flop
- J-K Flip-Flop
- D Flip-Flop
- T Flip-Flop

8.2.2.1 S-R Flip-Flop

This simple flip-flop circuit has a set input (S) and a reset input (R). In this system, when you Set "S" as active the output "Q" would be high and "Q'" will be low. Once the outputs are established, the wiring of the circuit is maintained until "S" or "R" go high, or power is turned off. As shown above, it is the simplest and easiest to understand. The two outputs, as shown above, are the inverse of each other. The truth table of SR Flip-Flop is highlighted below.

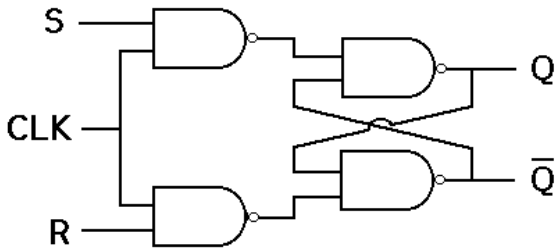


Figure 8.5 S-R Flip-Flop

Table 8.1 S-R Flip flop table

S	R	Q	Q'
0	0	0	1
0	1	0	1
1	0	1	0
1	1	∞	∞

8.2.2.2 J-K Flip-Flop

Due to the undefined state in the SR flip-flop, another flip-flop is required in electronics. The JK flip-flop is an improvement on the SR flip-flop where S=R=1 is not a problem.

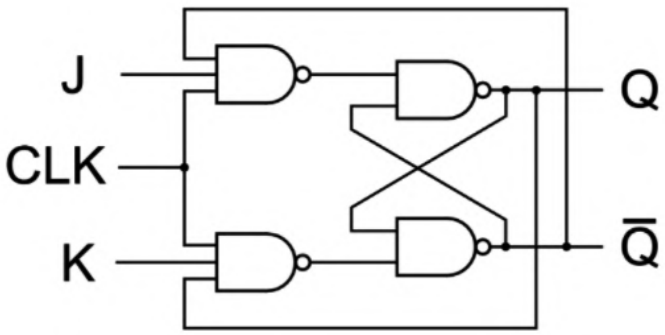


Figure 8.6 J-K Flip flop

The input condition of J=K=1, gives an output inverting the output state. However, the outputs are the same when one tests the circuit practically. In simple words, If J and K data input are different (i.e. high and low) then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock

edge then the output will toggle from one state to the other. JK Flip-Flops can function as Set or Reset Flip-flops

Table 8.2 J-K Flip flop truth table

J	K	Q	Q’
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	1
0	0	1	1
0	1	1	0
1	0	1	1
1	1	1	0

8.2.2.3 D Flip-Flop

D flip-flop is a better alternative that is very popular with digital electronics. They are commonly used for counters and shift-registers and input synchronization.

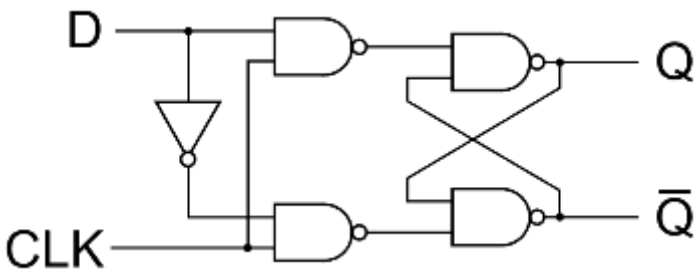


Figure 8.7 D Flip-Flop

In this, the output can be only changed at the clock edge, and if the input changes at other times, the output will be unaffected.

Table 8.3 D Flip-flop truth table

Clock	D	Q	Q’
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

The change of state of the output is dependent on the rising edge of the clock. The output (Q) is same as the input and can only change at the rising edge of the clock.

8.2.2.4 T Flip-Flop

A T flip-flop is like a JK flip-flop. These are basically a single input version of JK flip-flops. This modified form of JK flip-flop is obtained by connecting both inputs J and K together. It has only one input along with the clock input.

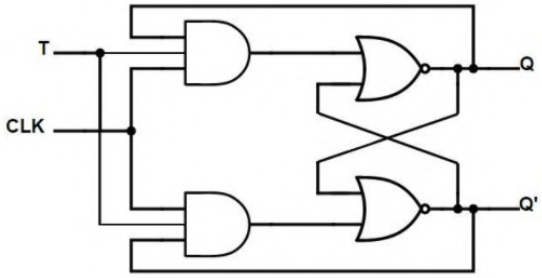


Figure 8.8 T- Flip Flop

These flip-flops are called T flip-flops because of their ability to complement its state (i.e.) Toggle, hence the name Toggle flip-flop.

Table 8.4 T-Flip flop truth table

T	Q	Q(t+1)
0	0	0
1	0	1
0	1	1
1	1	0

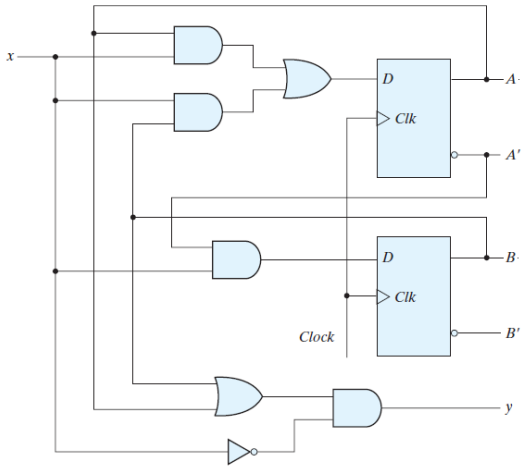
8.2.2.5 State Table:

The time sequence of inputs, outputs, and flip-flop states can be enumerated in a state table (some- times called a transition table). The table consists of four sections labeled present state, input, next state, and output. The present state section shows the states of flip-flops A and B at any given time t. The input section gives a value of x for each possible present state. The next state section shows the states of the flip-flops one clock cycle later, at time t+1. The output section gives the value of y at time t for each present state and input condition.

8.3 Analysis of Sequential Circuits

Behavior of a clocked sequential circuit is determined from the inputs, outputs, and the state of its flip-flops. Analysis of sequential circuit consists of obtaining a state table or a state diagram for the time sequence of inputs, outputs and internal states. Boolean expressions (State Equations) can also be used to describe the behavior of the sequential circuit.

Example:



- Input = x
- Output = y
- D Flip Flops

Time sequence of inputs, outputs, and flip-flop states can be enumerated in a state table (also called transition table). State Table is composed of three sections

- Present state
  Current State of Flip Flops at any given time t
- Next State
  Function of inputs, present state and type of F/F
- Output
  Output is described in terms of present state and input

State Table starts with an assumed initial state of Flip Flops. Flip Flop Inputs and Output (y)

$$D_A = Ax + Bx$$

$$D_B = A'x$$

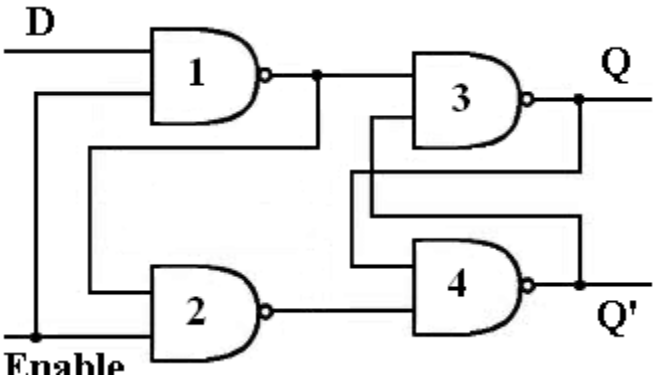
$$y = (A + B)x'$$

Present State		Next State				Output	
		$x = 0$		$x = 1$		$x = 0$	$x = 1$
A	B	A	B	A	B	y	y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

8.4 Lab Activities

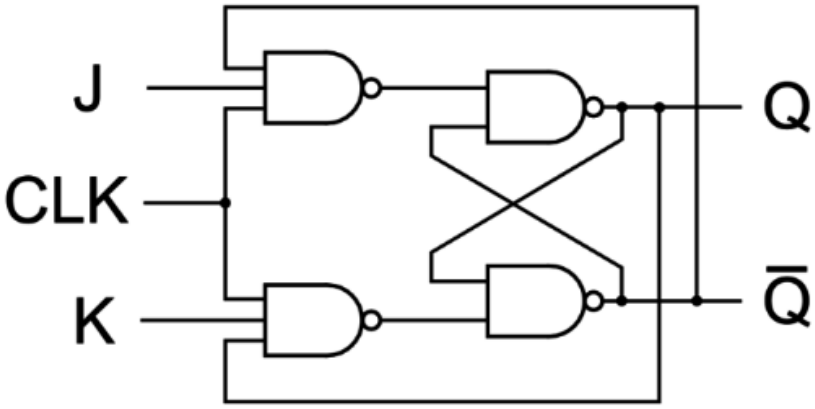
8.4.1 Task-1:

Implement D Latch and Perform Truth table base verification.



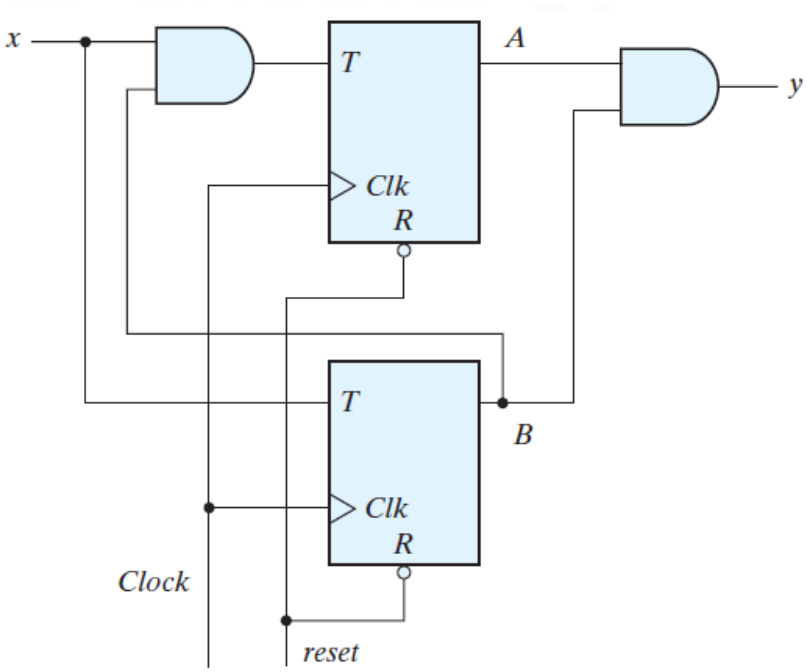
8.4.2 Task-2:

Implement J-K Flip Flop. Also Perform Truth Table based verification.



8.4.3 Task-3:

Implement the following sequential circuit and verify its state table.



Lab Exercise and Summary

Summary should cover Introduction, Procedure, Data Analysis and Evaluation.

Student's Signature: _____ **Date: _____**

LABORATORY SKILLS ASSESMENT (Psychomotor)

Total Marks: 100

Criteria (Max Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S< 70%	Level 3 70% ≤ S< 90%	Level 4 90%≤ S ≤100%	Score (S)
Procedural Awareness (20)	Selects inappropriate skills and/or strategies required by the task	Selects and applies appropriate skills and/or strategies required by the task with some errors	Selects and applies the appropriate strategies and/or skills specific to the task without significant errors	Selects and applies appropriate strategies and/or skills specific to the task without any error	
Practical Implementation (30)	Makes several critical errors in applying procedural knowledge of implementing D-type latch and J-K flip flop	Makes few critical errors in applying procedural knowledge of implementing D-type latch and J-K flip flop	Makes some non-critical errors in applying procedural knowledge of implementing D-type latch and J-K flip flop	Applies the procedural knowledge of implementing D-type latch and J-K flip flop in perfect ways	
Safety (10)	Requires constant reminders to follow safety procedures	Requires some reminders to follow safety procedures	Follows safety procedures with only minimal reminders	Routinely follows safety procedures	
Use of Tool/Equipment (20)	Uses tools, equipment and materials with limited competence	Uses tools, equipment and materials with some competence	Uses tools, equipment and materials with considerable competence	Uses tools, equipment and materials with a high degree of competence	
Participation to Achieve Group Goals (10)	Shows little commitment to group goals and fails to perform assigned roles	Demonstrates commitment to group goals, but has difficulty performing assigned roles	Demonstrates commitment to group goals and carries out assigned roles effectively	Actively helps to identify group goals and works effectively to meet them in all roles assumed	
Interpersonal Skills in Group Work (10)	Rarely interacts positively within a group, even with prompting	Interacts with other group members if prompted	Interacts with all group members spontaneously	Interacts positively with all group members and encourages such interaction in others	
				Marks Obtained	

Instructor's Signature: _____ **Date: _____**

LABORATORY SKILLS ASSESMENT (Affective)

Total Marks: 40

Criteria (Max. Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S < 70%	Level 3 70% ≤ S < 90%	Level 4 90% ≤ S ≤ 100%	Score (S)
Introduction (5)	Very little background information provided or information is incorrect	Introduction is brief with some minor mistakes	Introduction is nearly complete, missing some minor points	Introduction complete and well-written; provides all necessary background principles for the experiment	
Procedure (5)	Many stages of the procedure are not entered on the lab report.	Many stages of the procedure are entered on the lab report.	The procedure could be more efficiently designed but most stages of the procedure are entered on the lab report.	The procedure is well designed and all stages of the procedure are entered on the lab report.	
Data Record (10)	Data is brief and missing significant pieces of information.	Data provides some significant information and has few critical mistakes.	Data is almost complete but has some minor mistakes.	Data is complete and relevant. Tables with units are provided. Graphs are labeled. All questions are answered correctly.	
Data Analysis (10)	Data is presented in very unclear manner. Error analysis is not included.	Data is presented in ways (charts, tables, graphs) that are not clear enough. Error analysis is included.	Data is presented in ways (charts, tables, graphs) that can be understood and interpreted. Error analysis is included.	Data are presented in ways (charts, tables, graphs) that best facilitate understanding and interpretation. Error analysis is included.	
Report Quality (10)	Report contains many errors.	Report is somewhat organized with some spelling or grammatical errors.	Report is well organized and cohesive but contains some grammatical errors.	Report is well organized and cohesive and contains no grammatical errors. Presentation seems polished.	
				Marks Obtained	

LABORATORY SKILLS ASSESSMENT (Cognitive)

Total Marks: 10

(If any) **Marks Obtained**	

Instructor's Signature: _____ **Date: _____**