Experiment No 4

RISC-V assembly programming using Data Transfer and Arithmetic Instructions

4.1 Objectives

After completing this experiment, student will be able to:

- Gain proficiency in using data transfer instructions (**lw** and **sw**) to move data between memory and registers.
- Understand the syntax and functionality of data transfer instructions in RISC-V assembly programming.
- Explore arithmetic instructions (**add**, **sub**, **mul**, and **div**) for performing basic arithmetic operations on registers.
- Learn how to specify memory addresses and register operands in data transfer and arithmetic instructions.
- Practice writing RISC-V assembly code to load data from memory, perform arithmetic operations, and store results back into memory.
- Develop skills in debugging RISC-V assembly programs using the Venus IDE, including setting breakpoints, inspecting register values, and verifying program correctness.
- Enhance understanding of memory organization, register manipulation, and program execution flow in RISC-V architecture.

4.2 Background Theory

This lab on "RISC-V assembly programming using Data Transfer and Arithmetic Instructions in Venus" aims to provide students with a foundational understanding of low-level programming concepts within the RISC-V architecture. RISC-V, as an open-source instruction set architecture, offers a versatile platform for learning assembly language programming. Through this lab, students will explore the fundamentals of data transfer and arithmetic operations, essential for manipulating data within a RISC-V environment. By leveraging instructions like **lw** and **sw** for memory operations and **add**, **sub**, **mul**, and **div** for arithmetic computations, students will gain hands-on experience in moving data between registers and memory, performing basic arithmetic operations, and storing results back into memory. This lab not only familiarizes students with the syntax and usage of these instructions but also cultivates a deeper understanding of memory organization, register manipulation, and the execution flow of RISC-V programs. Through practical exercises conducted in the Venus IDE, students will develop proficiency in writing efficient and effective

RISC-V assembly code, laying a solid groundwork for further exploration into computer architecture and systems programming.

4.2.1.1 RISC-V Architecture

RISC-V, an open-source instruction set architecture (ISA), embodies the principles of simplicity and modularity, making it highly adaptable across a wide range of computing devices. It features a clean and elegant design with a small set of fixed-length instructions, categorized into base and optional extensions, allowing for flexibility and scalability. The architecture defines a set of registers, including general-purpose registers and special-purpose registers, providing a foundation for efficient data manipulation and control flow. RISC-V supports various addressing modes and instruction formats, facilitating ease of programming and efficient code generation. Its modular design allows for the inclusion of custom extensions tailored to specific application domains, promoting innovation and specialization. Overall, RISC-V architecture stands as a versatile and extensible framework, poised to drive innovation in computing across diverse applications and industries.

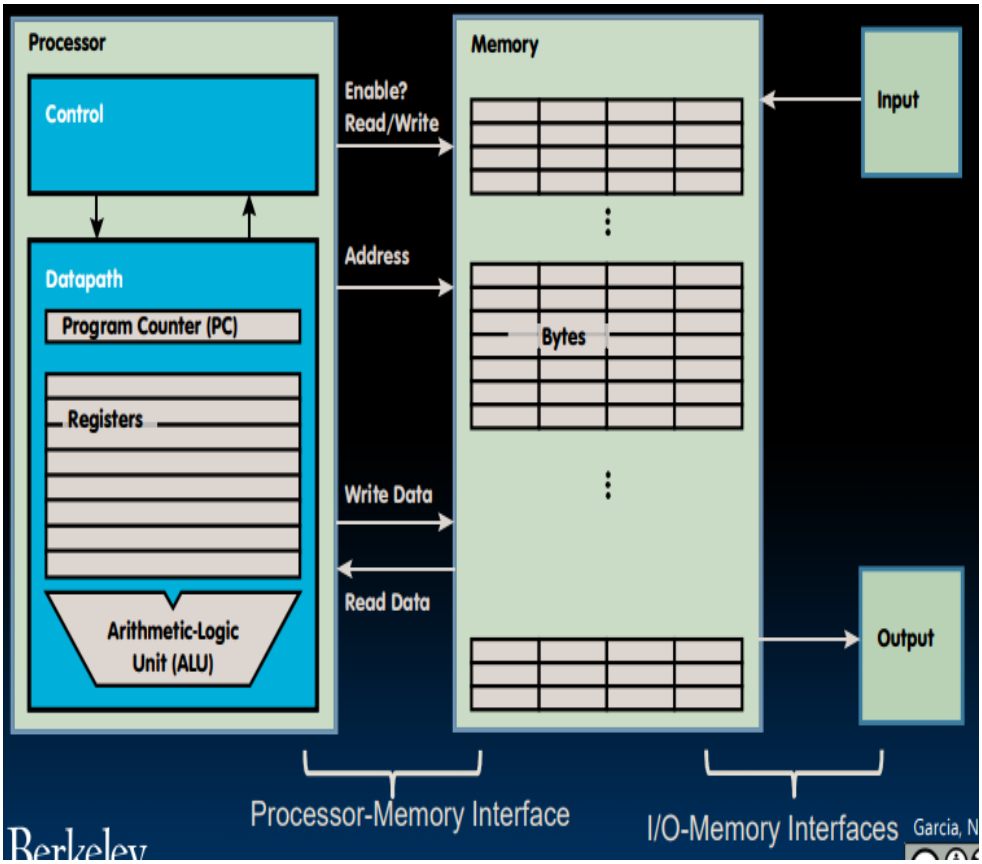


Figure 4.1: RISC-V Architecture

4.2.1.2 Basics of RISC-V assembly programming

Following are the foundational concepts and instructions for writing RISC-V assembly programs. By combining these elements, you can create programs to perform various computational tasks, manipulate data, control program flow, and interact with memory. Practice with these basics will help you gain proficiency in RISC-V assembly programming.

4.2.1.2.1 Registers

- RISC-V architecture includes 32 general-purpose registers (**x0** to **x31**) and a few special-purpose registers like the program counter (**pc**) and the stack pointer (**sp**).
- Example: Loading a value into a register and storing it in memory:

```assembly
li x1, 42      # Load immediate value 42 into register x1
sw x1, 0(x2)   # Store value in x1 into memory at address stored in x2
```

4.2.1.2.2 Data Transfer Instructions

- **lw** (load word) loads a 32-bit value from memory into a register.
- **sw** (store word) stores a 32-bit value from a register into memory.
- Example:

```
lw x3, 100(x4)   # Load value from memory into register x3
sw x5, 200(x6)   # Store value from register x5 into memory
```

4.2.1.2.3 Arithmetic Instructions

- **add** adds two registers and stores the result in another register.
- **sub** subtracts one register from another and stores the result in another register.
- Example:

```
add x7, x8, x9   # Add values in x8 and x9, store result in x7
sub x10, x11, x12 # Subtract value in x12 from x11, store result in x10
```

Multiplication:

- Load the first operand (**operand1**) into register **t0** using the **lw** instruction.
- Load the second operand (**operand2**) into register **t1** using the **lw** instruction.
- Multiply the values in registers **t0** and **t1** using the **mul** instruction, and store the result in register **t2**.
- Store the result from register **t2** into memory using the **sw** instruction.
- Example:

```
.data
    operand1:   .word 5      # Define operand1 as 5
    operand2:   .word 8      # Define operand2 as 8
    result:     .word 0      # Define a space to store the result

.text
    lw  t0, operand1   # Load operand1 into register t0
    lw  t1, operand2   # Load operand2 into register t1
    mul t2, t0, t1     # Multiply operand1 and operand2, store result in t2
    sw  t2, result     # Store the result in memory
```

Division:

- Load the dividend (**dividend**) into register **a0** using the **lw** instruction.
- Load the divisor (**divisor**) into register **a1** using the **lw** instruction.
- Divide the value in register **a0** by the value in register **a1** using the **div** instruction. The quotient is stored in the special register **lo**.
- Move the quotient from the special register **lo** to a general-purpose register **t3** using the **mflo** instruction.
- Store the quotient from register **t3** into memory using the **sw** instruction.
- Example:

```
.data
    dividend:    .word 20      # Define dividend as 20
    divisor:     .word 5       # Define divisor as 5
    quotient:    .word 0       # Define a space to store the quotient

.text
    lw  a0, dividend    # Load dividend into register a0
    lw  a1, divisor     # Load divisor into register a1
    div a0, a1          # Divide dividend by divisor, quotient stored in a0
    mflo t3             # Move the quotient from lo register to t3
    sw  t3, quotient    # Store the quotient in memory
```

4.2.1.2.4 Labeling and Comments

- Labels are used to mark specific locations in the code, facilitating branching and jumping.
- Comments provide explanatory notes within the code.
- Example:

```
loop_start:
    addi x18, x18, 1    # Increment x18
    bne x18, x19, loop_start    # Branch back to loop_start if x18 != x19
```

4.2.1.2.5 Data Directives

- **.data** directive marks the beginning of the data section, where data is initialized.
- **.word** directive allocates memory for a 32-bit word and initializes it with specified values.
- Example:

```
.data
my_data: .word 42, 56, -10   # Define an array of three 32-bit integers
```

RISC-V operands

Name	Example	Comments
32 registers	x0-x31	Fast locations for data. In RISC-V, data must be in registers to perform arithmetic. Register x0 always equals 0.
2^{30} memory words	Memory[0], Memory[4], ..., Memory[4,294,967,292]	Accessed only by data transfer instructions. RISC-V uses byte addresses, so sequential word accesses differ by 4. Memory holds data structures, arrays, and spilled registers.

Figure 4.2: RISC-V Operands

RISC-V assembly language

Category	Instruction	Example	Meaning	Comments
Arithmetic	Add	add x5, x6, x7	x5 = x6 + x7	Three register operands; add
	Subtract	sub x5, x6, x7	x5 = x6 - x7	Three register operands; subtract
	Add immediate	addi x5, x6, 20	x5 = x6 + 20	Used to add constants
Data transfer	Load word	lw x5, 40(x6)	x5 = Memory[x6 + 40]	Word from memory to register
	Load word, unsigned	lwu x5, 40(x6)	x5 = Memory[x6 + 40]	Unsigned word from memory to register
	Store word	sw x5, 40(x6)	Memory[x6 + 40] = x5	Word from register to memory
	Load halfword	lh x5, 40(x6)	x5 = Memory[x6 + 40]	Halfword from memory to register
	Load halfword, unsigned	lhu x5, 40(x6)	x5 = Memory[x6 + 40]	Unsigned halfword from memory to register
	Store halfword	sh x5, 40(x6)	Memory[x6 + 40] = x5	Halfword from register to memory
	Load byte	lb x5, 40(x6)	x5 = Memory[x6 + 40]	Byte from memory to register
	Load byte, unsigned	lbu x5, 40(x6)	x5 = Memory[x6 + 40]	Byte unsigned from memory to register
	Store byte	sb x5, 40(x6)	Memory[x6 + 40] = x5	Byte from register to memory
	Load reserved	lr.d x5, (x6)	x5 = Memory[x6]	Load; 1st half of atomic swap
	Store conditional	sc.d x7, x5, (x6)	Memory[x6] = x5; x7 = 0/1	Store; 2nd half of atomic swap
	Load upper immediate	lui x5, 0x12345	x5 = 0x12345000	Loads 20-bit constant shifted left 12 bits
Logical	And	and x5, x6, x7	x5 = x6 & x7	Three reg. operands; bit-by-bit AND
	Inclusive or	or x5, x6, x8	x5 = x6 | x8	Three reg. operands; bit-by-bit OR
	Exclusive or	xor x5, x6, x9	x5 = x6 ^ x9	Three reg. operands; bit-by-bit XOR
	And immediate	andi x5, x6, 20	x5 = x6 & 20	Bit-by-bit AND reg. with constant
	Inclusive or immediate	ori x5, x6, 20	x5 = x6 | 20	Bit-by-bit OR reg. with constant
	Exclusive or immediate	xori x5, x6, 20	x5 = x6 ^ 20	Bit-by-bit XOR reg. with constant
Shift	Shift left logical	sll x5, x6, x7	x5 = x6 << x7	Shift left by register
	Shift right logical	srl x5, x6, x7	x5 = x6 >> x7	Shift right by register
	Shift right arithmetic	sra x5, x6, x7	x5 = x6 >> x7	Arithmetic shift right by register
	Shift left logical immediate	slli x5, x6, 3	x5 = x6 << 3	Shift left by immediate
	Shift right logical immediate	srli x5, x6, 3	x5 = x6 >> 3	Shift right by immediate
	Shift right arithmetic immediate	srai x5, x6, 3	x5 = x6 >> 3	Arithmetic shift right by immediate
Conditional branch	Branch if equal	beq x5, x6, 100	if (x5 == x6) go to PC+100	PC-relative branch if registers equal
	Branch if not equal	bne x5, x6, 100	if (x5 != x6) go to PC+100	PC-relative branch if registers not equal
	Branch if less than	blt x5, x6, 100	if (x5 < x6) go to PC+100	PC-relative branch if registers less
	Branch if greater or equal	bge x5, x6, 100	if (x5 >= x6) go to PC+100	PC-relative branch if registers greater or equal
	Branch if less, unsigned	bltu x5, x6, 100	if (x5 < x6) go to PC+100	PC-relative branch if registers less, unsigned
	Branch if greater or equal, unsigned	bgeu x5, x6, 100	if (x5 >= x6) go to PC+100	PC-relative branch if registers greater or equal, unsigned
Unconditional branch	Jump and link	jal x1, 100	x1 = PC+4; go to PC+100	PC-relative procedure call
	Jump and link register	jalr x1, 100(x5)	x1 = PC+4; go to x5+100	Procedure return; indirect call

Figure 4.3: RISC-V Assembly Language

4.2.2 Venus IDE

Venus IDE provides a user-friendly environment for learning and practicing RISC-V assembly programming, including data transfer and arithmetic instructions. Here's an explanation of how Venus IDE facilitates RISC-V programming using these instructions:

4.2.2.1 Code Editor

Venus offers a built-in code editor where users can write RISC-V assembly code. The editor provides syntax highlighting, auto-indentation, and line numbering features, enhancing code readability and ease of writing.

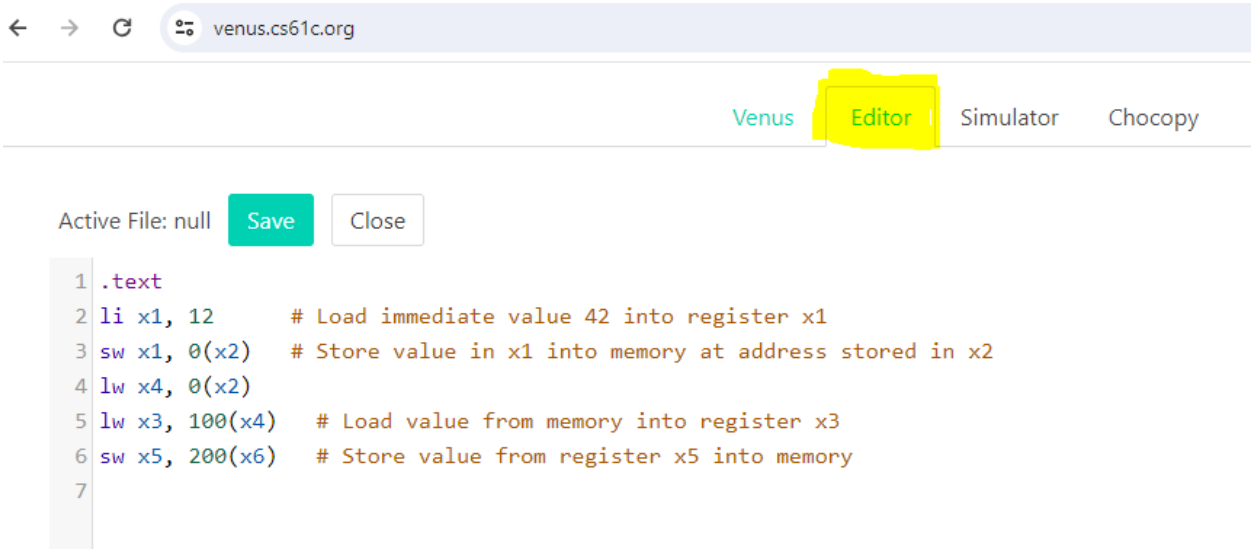


Figure 4.4: Editor

4.2.2.2 Assembler

Venus includes an assembler that translates RISC-V assembly code written in the editor into machine code. When the user clicks on the "Assemble" button, the assembler processes the code, checks for syntax errors, and generates the corresponding machine code.

4.2.2.3 Simulator

After assembling the code, Venus provides a simulation environment where users can execute their RISC-V programs step-by-step. The simulator allows users to observe the effects of each instruction on the CPU state, including register values, memory contents, and program counter (PC) changes.

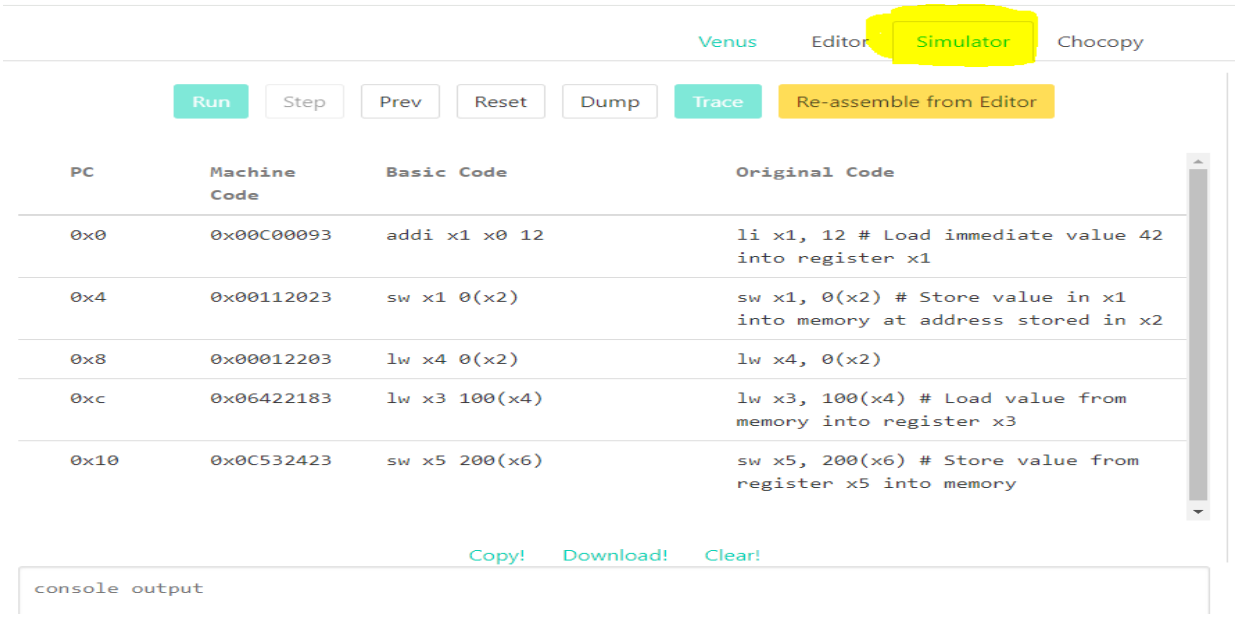


Figure 4.5: Simulator

4.2.2.4 Debugger

Venus comes equipped with a debugger that helps users troubleshoot and analyze their RISC-V programs. Users can set breakpoints, inspect register and memory values, and step through the code to identify logic errors or unexpected behavior.

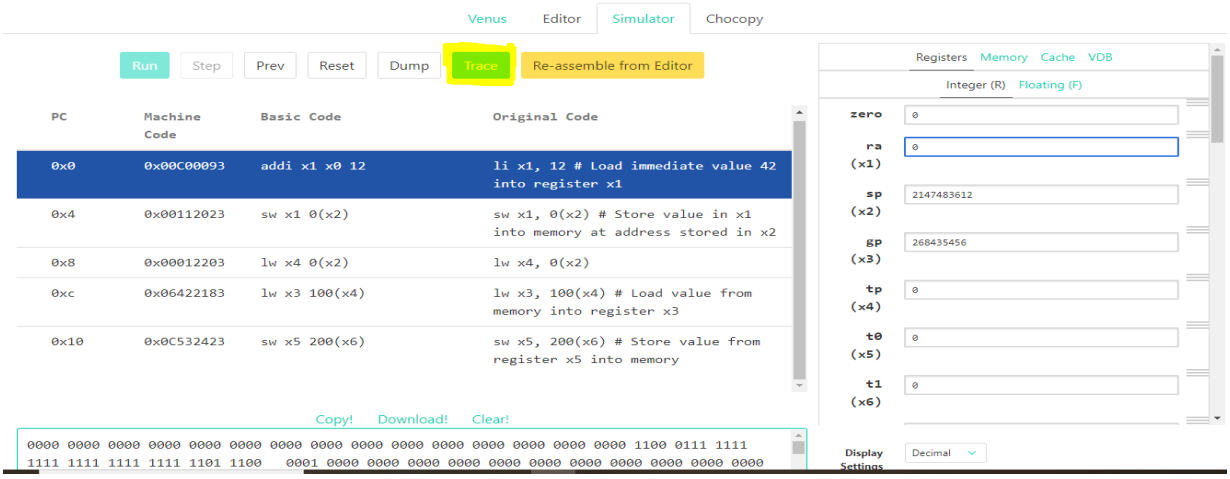


Figure 4.6: Trace

4.2.2.5 Memory Visualization

Venus provides a memory visualization feature that allows users to view the contents of memory locations as they execute their programs. This feature helps users track the data being transferred between memory and registers during data transfer instructions.

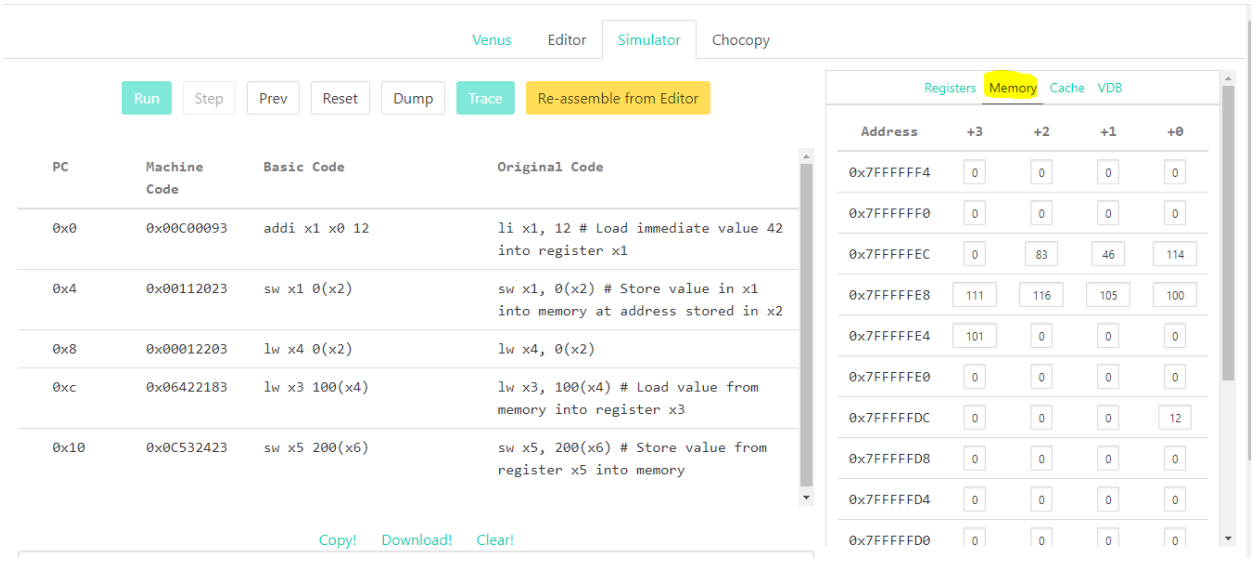


Figure 4.7: Memory Visualization

4.2.2.6 Register Display

Venus displays the current values of CPU registers, including general-purpose registers (x0 to x31) and special-purpose registers (pc, sp, etc.). Users can monitor register values to verify the correctness of arithmetic operations and data transfers.

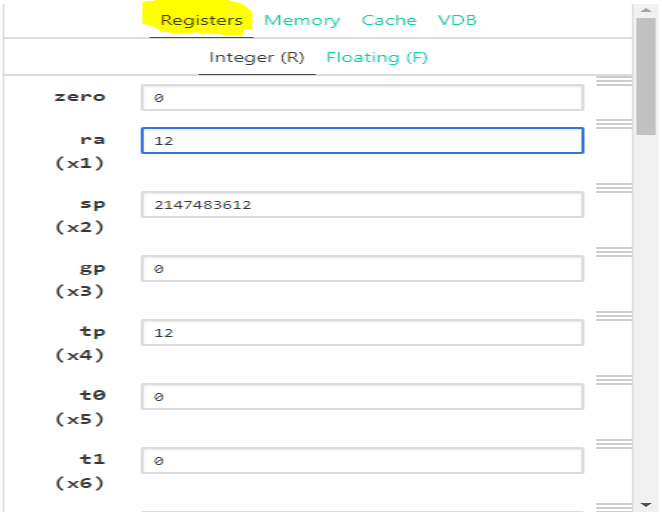


Figure 4.1: Register Display

4.2.2.7 Example Programs

Venus includes a collection of example programs demonstrating various RISC-V assembly programming concepts, including data transfer and arithmetic instructions. Users can study these examples to understand how to use these instructions effectively in their own programs.

4.3 Lab Activities

4.3.1 Task-1 Write a RISC-V assembly program to manipulate data using data transfer instructions in the Venus IDE. Your program should perform the following tasks:

1. Load an array of integers from memory into registers using the **lw** instruction.
2. Calculate the sum of all integers in the array and store the result in a designated register.
3. Store the computed sum back into memory at a specific memory location using the **sw** instruction.

Your task is to write the RISC-V assembly code to accomplish the above objectives and test it using the Venus IDE. Execute the program in the Venus simulator, and observe the values loaded from memory, the computed sum, and the stored result in registers.

Note: Add Screen shots of outputs and show it to instructor.

4.3.2 Task-2 Develop a RISC-V assembly program to demonstrate the use of arithmetic instructions in the Venus IDE. The program should accomplish the following objectives:

1. Perform addition and subtraction operations on predetermined values stored in registers using the **add** and **sub** instructions.
2. Implement multiplication and division operations between specified registers using the **mul** and **div** instructions.
3. Verify the correctness of the arithmetic operations by inspecting the results stored in registers.

4.3.3 Task-3 Develop a RISC-V assembly program in the Venus IDE that combines arithmetic and data transfer instructions to perform a simple computational task. The program should achieve the following objectives:

1. Load two integers from memory into registers using the lw instruction.
2. Perform an arithmetic operation (addition, subtraction, multiplication, or division) between the two integers using the corresponding arithmetic instruction (add, sub, mul, or div).
3. Store the result of the arithmetic operation back into memory at a specified memory location using the sw instruction.

Note: Show your outputs to your instructor.

Lab Exercise and Summary

Summary should cover Introduction, Procedure, Data Analysis and Evaluation.

Student's Signature: _____ **Date: _____**

Cognitive Activity

Answer both questions. Each question carries 5 marks.

Q1. Trace the following RISC-V code by hand and give the final value in register t2:

```
li t0, 5
li t1, 10
add t2, t0, t1
sw t2, 0(sp)
lw t3, 0(sp)
sub t2, t3, t0
```

(5)

Ans: _____

_____

_____

_____

_____

Q2. Write a short RISC-V assembly snippet (using lw, mul and sw) that loads two numbers from memory addresses 0(s0) and 4(s0), multiplies them, and stores the result back at address 8(s0). Explain each line briefly. **(5)**

Ans: _____

_____

_____

_____

_____

Obtained Marks	**/10**

Psychomotor Activity 1 — Experimental Setup

S. No	Criteria	Performance	Description	Marks
1	Tool Setup (4)	Level 4	Opens and configures Venus and selects the required environment correctly and independently.	4
		Level 3	Configures the required tool with minor errors or assistance.	3
		Level 2	Completes the setup with considerable assistance.	2
		Level 1	Setup is incomplete and requires substantial assistance.	1
2	File/Design Setup (4)	Level 4	Correctly creates/selects the required assembly file, Logisim circuit/design and required components for the RISC-V assembly program.	4
		Level 3	File/design setup is mostly correct with minor errors or omissions.	3
		Level 2	Setup is partially completed and requires assistance.	2
		Level 1	Major errors or omissions are present in the setup.	1
3	Parameter Setup (2)	Level 2	Correctly defines required data, registers, parameters, components and initial conditions.	2
		Level 1	Most required inputs/components are correctly configured with minor errors.	1
			Total Obtained	/10

If a student is absent:

Criteria	Description	Marks
Absent	Student is absent from the laboratory activity.	0

Psychomotor Activity 2 — Implementation + Results

S. No	Criteria	Performance	Description	Marks
1	**Implementation (4)**	Level 4	Implements the required RISC-V assembly program correctly and independently.	**4**
		Level 3	Implements the required program/design with minor errors or assistance.	**3**
		Level 2	Partially implements the program/design and requires considerable assistance.	**2**
		Level 1	Implementation is largely incomplete and requires substantial assistance.	**1**
2	**Execution/Simulation (2)**	Level 2	Executes the RISC-V program or simulates the Logisim design correctly and handles basic errors appropriately.	**2**
		Level 1	Executes/simulates the work with minor errors or assistance.	**1**
3	**Results/Output (4)**	Level 4	Obtains correct results and clearly demonstrates the required program output or circuit behavior.	**4**
		Level 3	Obtains mostly correct results with minor errors.	**3**
		Level 2	Obtains partially correct results with noticeable errors or omissions.	**2**
		Level 1	Results are largely incorrect or incomplete.	**1**
			Total Obtained	**/10**

If a student is absent:

Criteria	Description	Marks
Absent	Student is absent from the laboratory activity.	**0**

Affective Activity — Lab Report + Viva Voce

S. No	Criteria	Performance	Description	Marks
1	Lab Report Completeness & Organization (4)	Level 4	Report is complete, well organized and demonstrates full responsibility for the assigned work.	4
		Level 3	Report is complete with minor omissions or organizational issues and demonstrates satisfactory responsibility for the assigned work.	3
		Level 2	Report is partially complete with several omissions and demonstrates limited responsibility for the assigned work.	2
		Level 1	Report has major omissions or poor organization and demonstrates minimal responsibility for the assigned work.	1
2	Code/Design, Results & Conclusion (2)	Level 2	RISC-V assembly program, results, and conclusion are correctly presented and discussed, demonstrating ownership of the assigned work.	2
		Level 1	RISC-V assembly program, results, or conclusion are presented with minor errors or omissions.	1
3	Viva Voce (4)	Level 4	Clearly explains the assigned RISC-V assembly program, working, and results, demonstrating individual responsibility, participation, and effective communication.	4
		Level 3	Explains most of the assigned program/design and results correctly, with minor difficulty, and demonstrates good individual participation.	3
		Level 2	Explains basic aspects of the assigned program/design with some prompting and demonstrates basic participation.	2
		Level 1	Demonstrates limited understanding or involvement and requires substantial prompting to explain the assigned work.	1
			Total Obtained	/10

The student has not submitted the report and has not appeared in the Viva Voce.

Criteria	Description	Marks
Lab Report and Results Not Submitted	Student has not submitted the report and results file.	**0**
Absent in Viva Voce	Student is absent from the viva voce.	**0**

Instructor's Signature: _____ **Date:** _____